1 GSPS Direct Digital Synthesizer with 14-Bit DAC

AD9912

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz output directly)
- Integrated 1 GSPS 14-bit DAC
- 48-bit frequency tuning word with 4 µHz resolution
- Differential HSTL comparator
- Flexible system clock input accepts either crystal or external reference clock
- On-chip low noise PLL REFCLK multiplier
- 2 SpurKiller channels
- Low jitter clock doubler for frequencies up to 750 MHz
- Single-ended CMOS comparator; frequencies < 150 MHz
- Programmable output divider for CMOS output
- Serial I/O control
- Excellent dynamic performance
- Software controlled power-down
- 64-lead LFCSP package
- Residual phase noise @ 250 MHz
  - 10 Hz offset: −113 dBc/Hz
  - 1 kHz offset: −133 dBc/Hz
  - 100 kHz offset: −153 dBc/Hz
  - 40 MHz offset: −161 dBc/Hz

APPLICATIONS

- Agile LO frequency synthesis
- Low jitter, fine tune clock generation
- Test and measurement equipment
- Wireless base stations, controllers
- Secure communications
- Fast frequency hopping

GENERAL DESCRIPTION

The AD9912 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC. The AD9912 features a 48-bit frequency tuning word (FTW), which can synthesize frequencies in step sizes no larger than 4 µHz. Absolute frequency accuracy can be achieved by adjusting the DAC system clock.

The AD9912 also features an integrated system clock PLL, which allows for system clock inputs as low as 25 MHz.

The AD9912 operates over an industrial temperature range, spanning −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

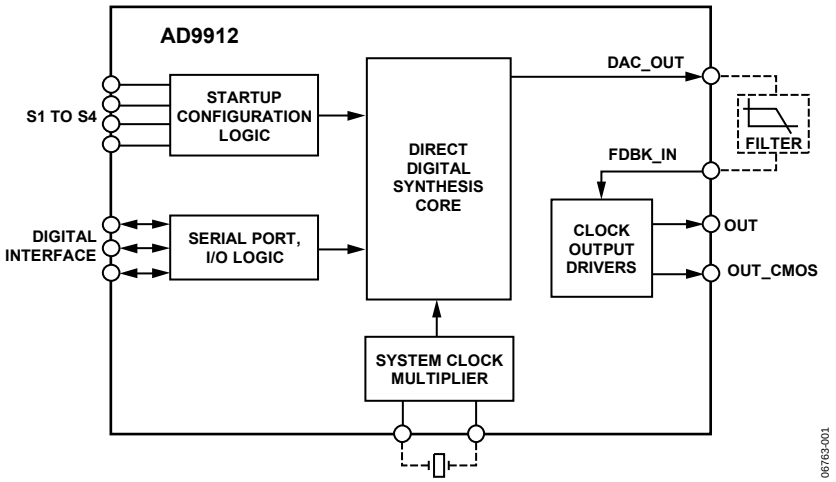

Figure 1. Basic Block Diagram

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10/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

Unless otherwise noted, AVDD = 1.8 V ± 5%, AVDD3 = 3.3 V ± 5%, DVDD = 1.8 V ± 5%, DVDD_I/O = 3.3 V ± 5%, AVSS = 0 V, DVSS = 0 V.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O (Pin 1)	3.135	3.30	3.465	V	
DVDD (Pin 3, Pin 5, Pin 7)	1.71	1.80	1.89	V	
AVDD3 (Pin 14, Pin 46, Pin 47, Pin 49)	3.135	3.30	3.465	V	
AVDD3 (Pin 37)	1.71	3.30	3.465	V	Pin 37 is typically 3.3 V, but can be set to 1.8 V
AVDD (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45, Pin 53)	1.71	1.80	1.89	V	
SUPPLY CURRENT					See also "Total Power Dissipation" specifications
I_{AVDD3} (Pin 37)		8	9.6	mA	CMOS output driver at 3.3 V, 50 MHz, with 5 pF load
I_{AVDD3} (Pin 46, Pin 47, Pin 49)		26	31	mA	DAC output current source, f_S = 1 GSPS
I_{AVDD} (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45)		113	136	mA	Aggregate analog supply, with system clock PLL, HSTL output driver, and S-divider enabled
I_{AVDD} (Pin 53)		40	48	mA	DAC power supply
I_{DVDD} (Pin 3, Pin 5, Pin 7)		205	246	mA	Digital core (SpurKiller off)
$I_{DVDD\_I/O}$ (Pin 1, Pin 14[1])		2	3	mA	Digital I/O (varies dynamically)
LOGIC INPUTS (Except Pin 32)					Pin 58 to Pin 61, Pin 64, Pin 9, Pin 10, Pin 54, Pin 55, Pin 63
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})	DVSS		0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CLKMODESEL (Pin 32) LOGIC INPUT					Pin 32 only
Input High Voltage (V_{IH})	1.4		AVDD	V	
Input Low Voltage (V_{IL})	AVSS		0.4	V	
Input Current (I_{INH}, I_{INL})		−18	−50	µA	At V_{IN} = 0 V and V_{IN} = AVDD
Maximum Input Capacitance (C_{IN})		3		pF	
LOGIC OUTPUTS					Pin 62 and bidirectional Pin 9, Pin 10, Pin 54, Pin 55, Pin 63
Output High Voltage (V_{OH})	2.7		DVDD	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})	DVSS		0.4	V	I_{OL} = 1 mA
FDBK INPUT					Pin 40, Pin 41
Input Capacitance		3		pF	
Input Resistance	18	22	26	kΩ	Differential
Differential Input Voltage Swing	225			mV p-p	Equivalent to 112.5 mV swing on each leg; must be ac-coupled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK INPUT					System clock inputs should always be ac-coupled (both single-ended and differential)
SYSCLK PLL Bypassed					
Input Capacitance		1.5		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.9	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing	632			mV p-p	Equivalent to 316 mV swing on each leg
SYSCLK PLL Enabled					
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.9	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing	632			mV p-p	Equivalent to 316 mV swing on each leg
Crystal Resonator with SYSCLK PLL Enabled					
Motional Resistance		9	100	Ω	25 MHz, 3.2 mm × 2.5 mm AT cut
CLOCK OUTPUT DRIVERS					
HSTL Output Driver					
Differential Output Voltage Swing	1080	1280	1480	mV	Output driver static, see Figure 27 for output swing vs. frequency
Common-Mode Output Voltage[2]	0.7	0.88	1.06	V	
CMOS Output Driver					Output driver static, see Figure 29 for output swing vs. frequency
Output Voltage High (V_{OH}) AVDDx = 3.3 V	2.7			V	I_{OH} = 1 mA
Output Voltage Low (V_{OL}) AVDDx = 3.3 V			0.4	V	I_{OL} = 1 mA
Output Voltage High (V_{OH}) AVDDx = 1.8 V	1.4			V	I_{OH} = 1 mA
Output Voltage Low (V_{OL}) AVDDx = 1.8 V			0.4	V	I_{OL} = 1 mA
TOTAL POWER DISSIPATION					
DDS Only		637	765	mW	Power-on default, except SYSCLK PLL bypassed and CMOS driver off; SYSCLK = 1 GHz; HSTL driver off; spur reduction off; f_{OUT} = 200 MHz
DDS with Spur Reduction On		686	823	mW	Same as "DDS Only" case, except both spur reduction channels on
DDS with HSTL Driver Enabled		657	788	mW	Same as "DDS Only" case, except HSTL driver enabled
DDS with CMOS Driver Enabled		729	875	mW	Same as "DDS Only" case, except CMOS driver and S-divider enabled and at 3.3 V; CMOS f_{OUT} = 50 MHz (S-divider = 4)
DDS with HSTL and CMOS Drivers Enabled		747	897	mW	Same as "DDS Only" case, except both HSTL and CMOS drivers enabled; S-divider enabled and set to 4; CMOS f_{OUT} = 50 MHz
DDS with SYSCLK PLL Enabled		648	777	mW	Same as "DDS Only" case, except 25 MHz on SYCLK input and PLL multiplier = 40
Power-Down Mode		13	16	mW	Using either the Power-Down and Enable register or the PWRDOWN pin

[1] Pin 14 is in the AVDD3 group, but it is recommended to tie Pin 14 to Pin 1.
[2] AVSS = 0 V.

AC SPECIFICATIONS

Unless otherwise noted, f_S = 1 GHz. DAC R_{SET} = 10 kΩ. Power supply pins within the range specified in the DC Specifications section.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FDBK INPUT					Pin 40, Pin 41
Input Frequency Range	10		400	MHz	
Minimum Differential Input Level	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled
	40			V/µs	
SYSTEM CLOCK INPUT					Pin 27, Pin 28
SYSCLK PLL Bypassed					
Input Frequency Range	250		1000	MHz	Maximum f_{OUT} is 0.4 × f_{SYSCLK}
Duty Cycle	45		55	%	
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
SYSCLK PLL Enabled					
VCO Frequency Range, Low Band	700		810	MHz	When in the range, use the low VCO band exclusively
VCO Frequency Range, Auto Band	810		900	MHz	When in the range, use the VCO auto band select
VCO Frequency Range, High Band	900		1000	MHz	When in the range, use the high VCO band exclusively
Maximum Input Rate of System Clock PFD			100	MHz	
Without SYSCLK PLL Doubler					
Input Frequency Range	11		200	MHz	
Multiplication Range	4		66		Integer multiples of 2, maximum PFD rate and system clock frequency must be met
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
With SYSCLK PLL Doubler					
Input Frequency Range	6		100	MHz	
Multiplication Range	8		132		Integer multiples of 8
Input Duty Cycle		50		%	Deviating from 50% duty cycle may adversely affect spurious performance
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
Crystal Resonator with SYSCLK PLL Enabled					
Crystal Resonator Frequency Range	10		50	MHz	AT cut, fundamental mode resonator
Maximum Crystal Motional Resistance			100	Ω	See the SYSCLK Inputs section for recommendations
CLOCK DRIVERS					
HSTL Output Driver					
Frequency Range	20		725	MHz	See Figure 27 for maximum toggle rate
Duty Cycle	48		52	%	
Rise/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Jitter (12 kHz to 20 MHz)		1.5		ps	f_{OUT} = 155.52 MHz, 50 MHz system clock input (see Figure 12 through Figure 14 for test conditions)
HSTL Output Driver with 2× Multiplier					
Frequency Range	400		725	MHz	
Duty Cycle	45		55	%	
Rise/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Subharmonic Spur Level		−35		dBc	Without correction
Jitter (12 kHz to 20 MHz)		1.6		ps	f_{OUT} = 622.08 MHz, 50 MHz system clock input (see Figure 15 for test conditions)
CMOS Output Driver (AVDD3/Pin 37) @ 3.3 V					
Frequency Range	0.008		150	MHz	See Figure 29 for maximum toggle rate, S-divider should be used for low frequencies as the FDBK_IN minimum frequency is 10 MHz
Duty Cycle	45	55	65	%	With 20 pF load and up to 150 MHz
Rise/Fall Time (20% to 80%)		3	4.6	ns	With 20 pF load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS Output Driver (AVDD3/Pin 37) @ 1.8 V					
Frequency Range	0.008		40	MHz	See Figure 28 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 40 MHz
Rise/Fall Time (20% to 80%)		5	6.8	ns	With 20 pF load
DAC OUTPUT CHARACTERISTICS					
DCO Frequency Range (1st Nyquist Zone)	0		450	MHz	Minimum slew rate for FDBK_IN dictates the lower limit if using CMOS or HSTL outputs, the DAC lower limit is 0 Hz
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVSS)
Output Capacitance		5		pF	
Full-Scale Output Current		20	31.7	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	%FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVSS − 0.50	+0.5	AVSS + 0.50	V	Outputs connected to a transformer whose center tap is grounded
Wideband SFDR					See the Typical Performance Characteristics section
20.1 MHz Output		−79		dBc	0 MHz to 500 MHz
98.6 MHz Output		−67		dBc	0 MHz to 500 MHz
201.1 MHz Output		−61		dBc	0 MHz to 500 MHz
398.7 MHz Output		−59		dBc	0 MHz to 500 MHz
Narrow-Band SFDR					See the Typical Performance Characteristics section
20.1 MHz Output		−95		dBc	±250 kHz
98.6 MHz Output		−96		dBc	±250 kHz
201.1 MHz Output		−91		dBc	±250 kHz
398.7 MHz Output		−86		dBc	±250 kHz
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		15		µs	
Time Required to Leave Power-Down		18		µs	
Reset Assert to High-Z Time for S1 to S4 Configuration Pins		60		ns	Time from rising edge of RESET to high-Z on the S1, S2, S3, S4 configuration pins
SERIAL PORT TIMING SPECIFICATIONS					
SCLK Clock Rate ($1/t_{CLK}$)		25	50	MHz	Refer to Figure 56 for all write-related serial port parameters, maximum SCLK rate for readback is governed by t_{DV}
SCLK Pulse Width High, t_{HI}	8			ns	
SCLK Pulse Width Low, t_{LO}	8			ns	
SDO/SDIO to SCLK Setup Time, t_{DS}	1.93			ns	
SDO/SDIO to SCLK Hold Time, t_{DH}	1.9			ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			11	ns	Refer to Figure 54
CSB to SCLK Setup Time, t_S	1.34			ns	
CSB to SCLK Hold Time, t_H	−0.4			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	
PROPAGATION DELAY					
FDBK to HSTL Output Driver		2.8		ns	
FDBK to HSTL Output Driver with 2× Frequency Multiplier Enabled		7.3		ns	
FDBK to CMOS Output Driver		8.0		ns	S-divider bypassed
FDBK Through S-Divider to CMOS Output Driver		8.6		ns	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/O)	3.6 V
DAC Supply Voltage (DAC_VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C
Thermal Resistance[1]	
θ_{JA}	25.2°C/W typical
θ_{JB}	13.9°C/W typical
θ_{JC}	1.7°C/W typical

[1] The exposed pad on bottom of package must be soldered to ground to achieve the specified thermal performance. See the Typical Performance Characteristics section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

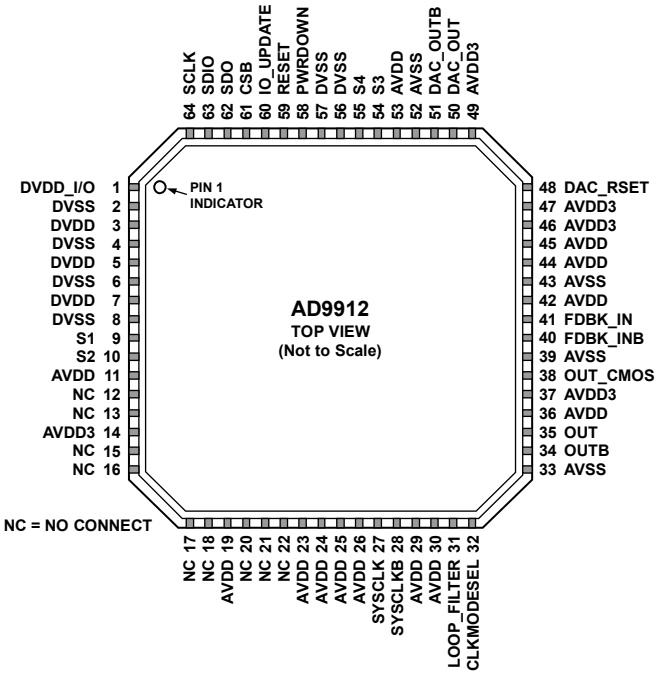

Figure 2. 64-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	I/O Digital Supply.
2, 4, 6, 8	I	Power	DVSS	Digital Ground. Connect to ground.
3, 5, 7	I	Power	DVDD	Digital Supply.
9, 10, 54, 55	I/O	3.3 V CMOS	S1, S2, S3, S4	Start-Up Configuration Pins. These pins are configured under program control and do not have internal pull-up/pull-down resistors.
11, 19, 23 to 26, 29, 30, 36, 42, 44, 45, 53	I	Power	AVDD	Analog Supply. Connect to a nominal 1.8 V supply.
12, 13, 15, 16, 17, 18, 20, 21, 22			NC	No Connect. These unused pins can be left unconnected.
14, 46, 47, 49	I	Power	AVDD3	Analog Supply. Connect to a nominal 3.3 V supply.
27	I	Differential Input	SYSCLK	System Clock Input. The system clock input has internal dc biasing and should always be ac-coupled, except when using a crystal. Single-ended 1.8 V CMOS can also be used, but can introduce a spur caused by an input duty cycle that is not 50%. When using a crystal, tie the CLKMODESEL pin to AVSS, and connect crystal directly to this pin and Pin 28.
28	I	Differential Input	SYSCLKB	Complementary System Clock. Complementary signal to the input provided on Pin 27. Use a 0.01 µF capacitor to ground on this pin if the signal provided on Pin 27 is single-ended.
31	O		LOOP_FILTER	System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed. See Figure 46 for a diagram of the system clock PLL loop filter.
32	I	1.8 V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source. This pin can be left unconnected when the system clock PLL is bypassed. (See the SYSCLK Inputs section for details on the use of this pin.)

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
33, 39, 43, 52	O	GND	AVSS	Analog Ground. Connect to ground.
34	O	1.8 V HSTL	OUTB	Complementary HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
35	O	1.8 V HSTL	OUT	HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
37	I	Power	AVDD3	Analog Supply for CMOS Output Driver. This pin is normally 3.3 V but can be 1.8 V. This pin should be powered even if the CMOS driver is not used. See the Power Supply Partitioning section for power supply partitioning.
38	O	3.3 V CMOS	OUT_CMOS	CMOS Output. See the Specifications section and the Output Clock Drivers and 2× Frequency Multiplier section. This pin is 1.8 V CMOS if Pin 37 is set to 1.8 V.
40	I	Differential Input	FDBK_INB	Complementary Feedback Input. When using the HSTL and CMOS outputs, this pin is connected to the filtered DAC_OUTB output. This internally biased input is typically ac-coupled, and when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
41	I	Differential Input	FDBK_IN	Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUT output.
48	O	Current Set Resistor	DAC_RSET	DAC Output Current Setting Resistor. Connect a resistor (usually 10 kΩ) from this pin to GND. See the DAC Output section.
50	O	Differential Output	DAC_OUT	DAC Output. This signal should be filtered and sent back on-chip through the FDBK_IN input. This pin has an internal 50 Ω pull-down resistor.
51	O	Differential Output	DAC_OUTB	Complimentary DAC Output. This signal should be filtered and sent back on-chip through the FDBK_INB input. This pin has an internal 50 Ω pull-down resistor.
56, 57		Power	DVSS	Digital Ground. Connect to ground.
58	I	3.3 V CMOS	PWRDOWN	Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power-down state. This pin has an internal 50 kΩ pull-down resistor.
59	I	3.3 V CMOS	RESET	Chip Reset. When this active high pin is asserted, the chip goes into reset. Note that on power-up, a 10 µs reset pulse is internally generated when the power supplies reach a threshold and stabilize. This pin should be grounded with a 10 kΩ resistor if not used.
60	I	3.3 V CMOS	IO_UPDATE	I/O Update. A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the Write section). This pin has an internal 50 kΩ pull-down resistor.
61	I	3.3 V CMOS	CSB	Chip Select. Active low. When programming a device, this pin must be held low. In systems where more than one AD9912 is present, this pin enables individual programming of each AD9912. This pin has an internal 100 kΩ pull-up resistor.
62	O	3.3 V CMOS	SDO	Serial Data Output. When the device is in 3-wire mode, data is read on this pin. There is no internal pull-up/pull-down resistor on this pin.
63	I/O	3.3 V CMOS	SDIO	Serial Data Input/Output. When the device is in 3-wire mode, data is written via this pin. In 2-wire mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
64	I	3.3 V CMOS	SCLK	Serial Programming Clock. Data clock for serial programming. This pin has an internal 50 kΩ pull-down resistor.
Exposed Die Pad	O	GND	AVSS	Analog Ground. Connect to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, AVDD, AVDD3, and DVDD at nominal supply voltage; DAC R_{SET} = 10 kΩ.
See Figure 26 for 1 GHz reference phase noise used for generating these plots.

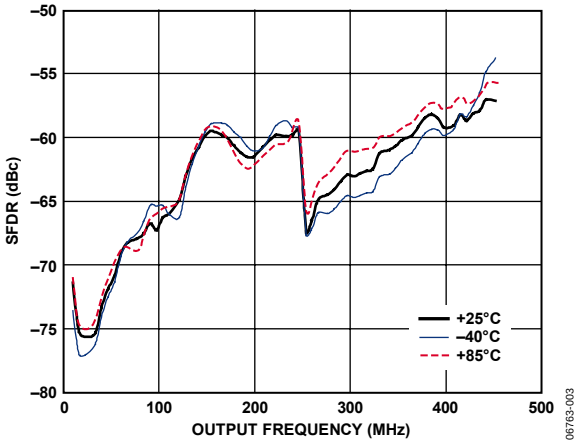

Figure 3. Wideband SFDR vs. Output Frequency at –40°C, +25°C, and +85°C, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

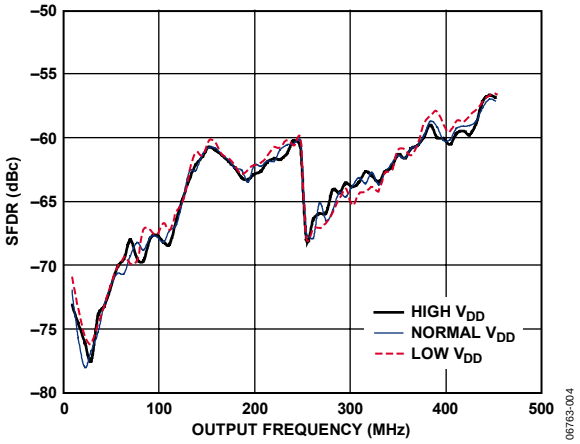

Figure 4. Variation of Wideband SFDR vs. Frequency over DAC Power Supply Voltage, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

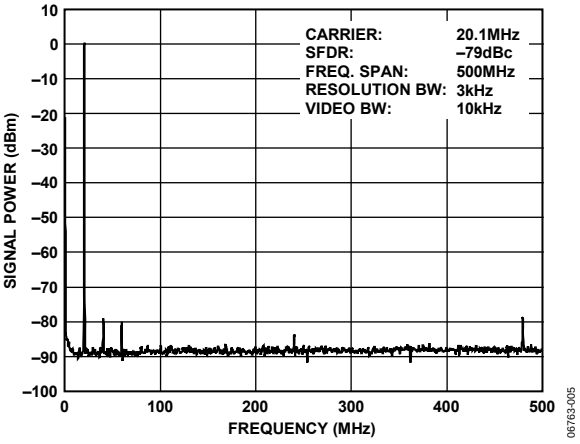

Figure 5. Wideband SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

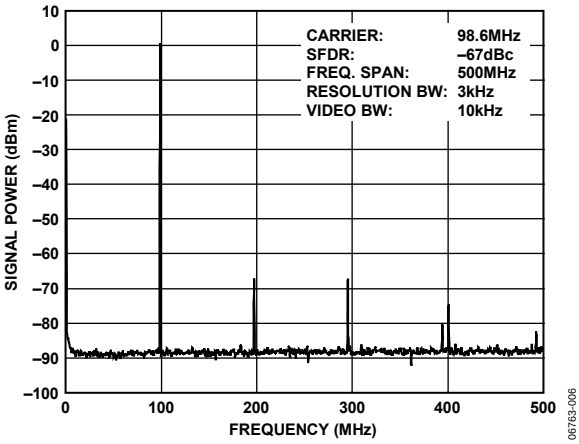

Figure 6. Wideband SFDR at 98.6 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

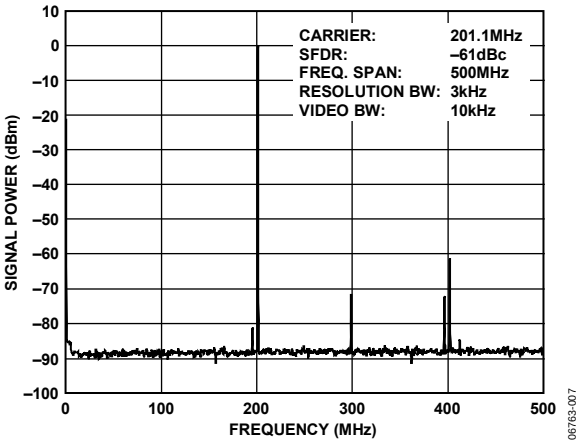

Figure 7. Wideband SFDR at 201.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

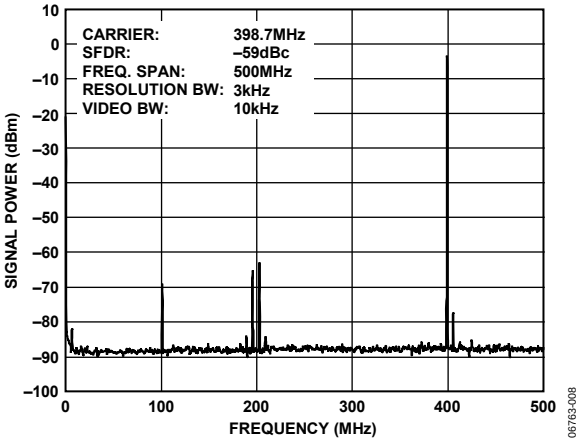

Figure 8. Wideband SFDR at 398.7 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

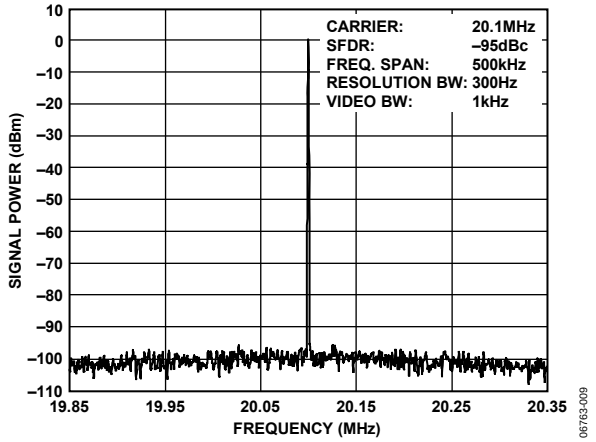

Figure 9. Narrow-Band SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

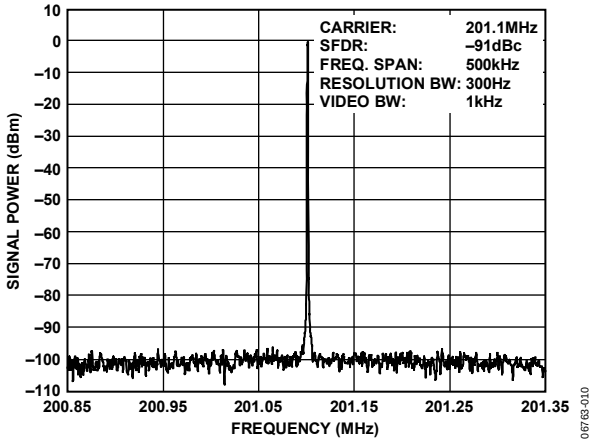

Figure 10. Narrow-Band SFDR at 201.1 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

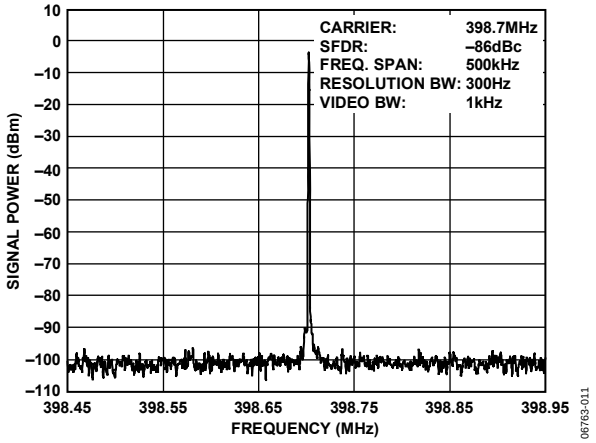

Figure 11. Narrow-Band SFDR at 398.7 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

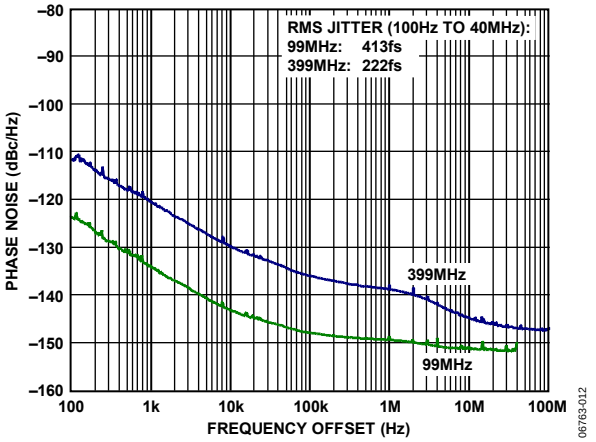

Figure 12. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

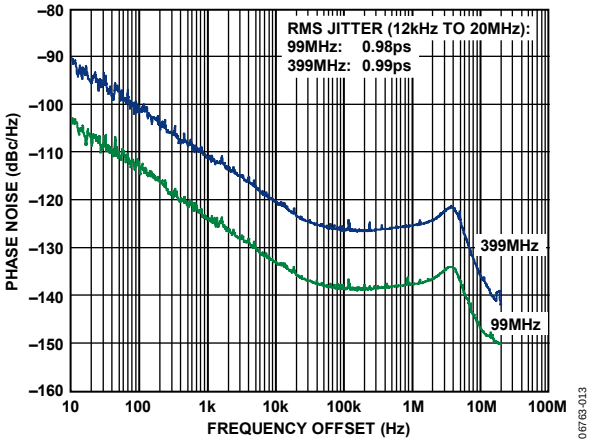

Figure 13. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 83.33 MHz)

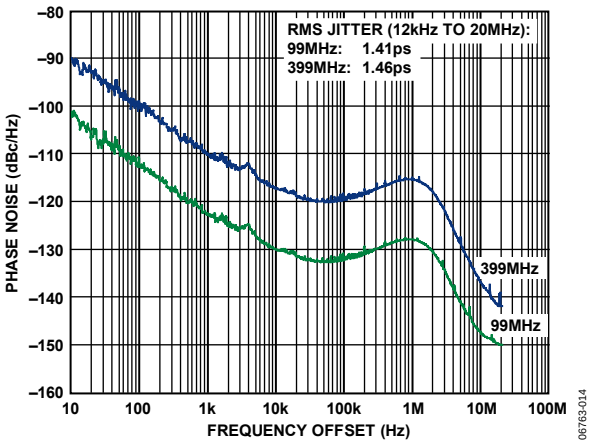

Figure 14. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 25 MHz)

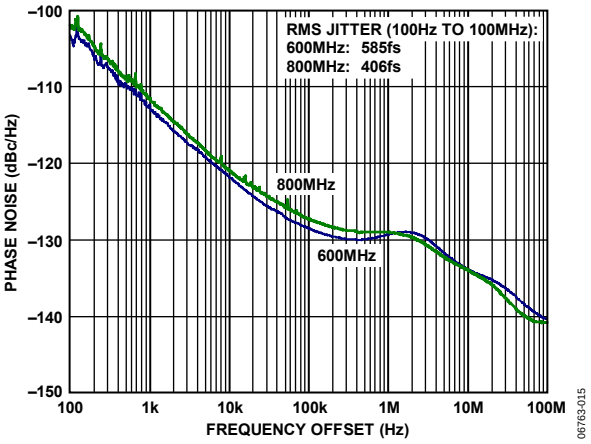

Figure 15. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed), HSTL Output Doubler Enabled

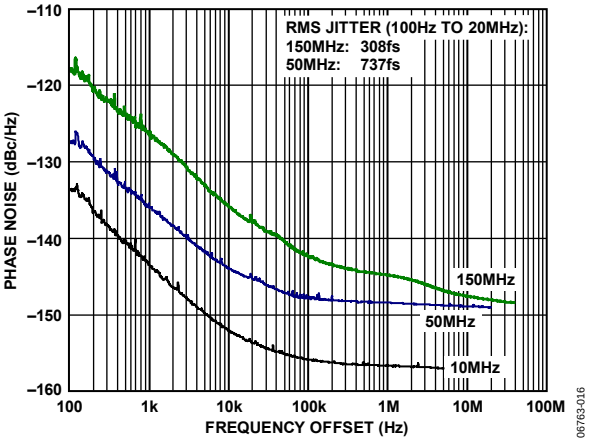

Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz Plot

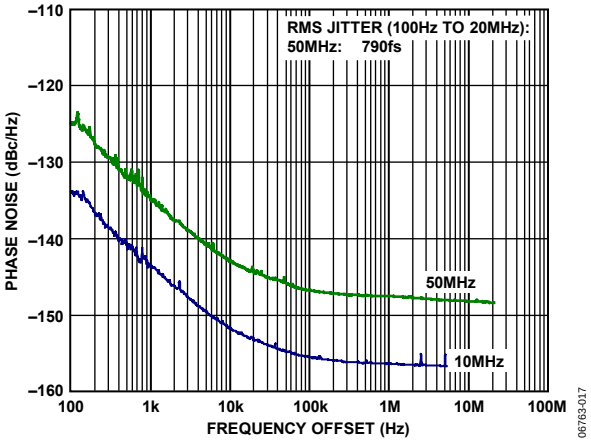

Figure 17. Absolute Phase Noise Using CMOS Driver at 1.8 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

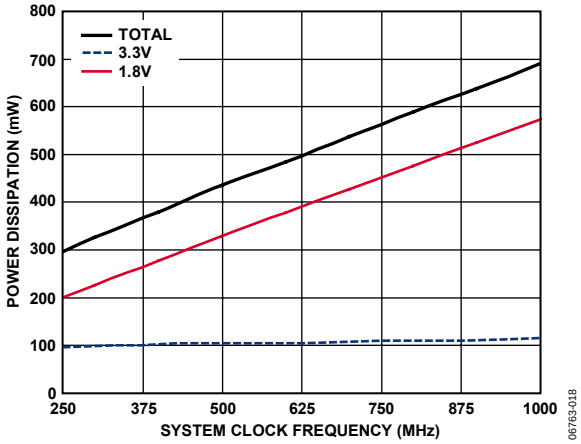

Figure 18. Power Dissipation vs. System Clock Frequency (SYSCLK PLL Bypassed), $f_{OUT} = f_{SYSCLK}/5$, HSTL Driver On, CMOS Driver On, SpurKiller Off

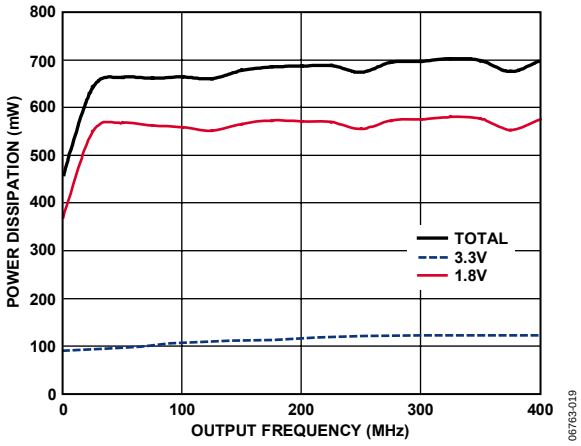

Figure 19. Power Dissipation vs. Output Frequency SYSCLK = 1 GHz (SYSCLK PLL Bypassed), HSTL Driver On, CMOS Driver On, SpurKiller Off

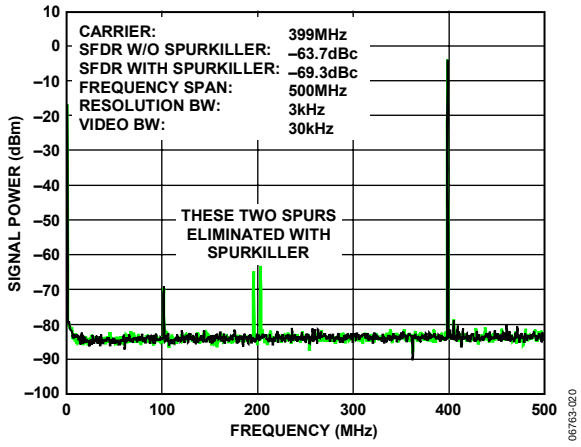

Figure 20. SFDR Comparison With and Without SpurKiller, SYSCLK = 1 GHz, f_{OUT} = 400 MHz

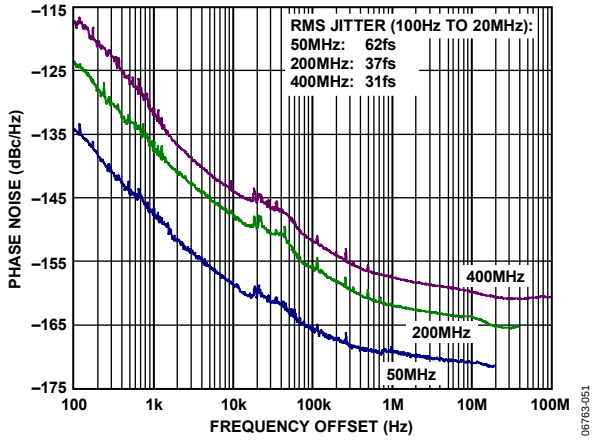

Figure 21. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 50 MHz, 200 MHz, and 400 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

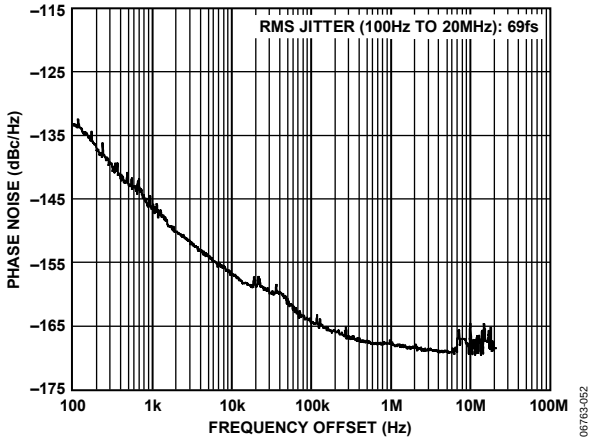

Figure 22. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 63 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

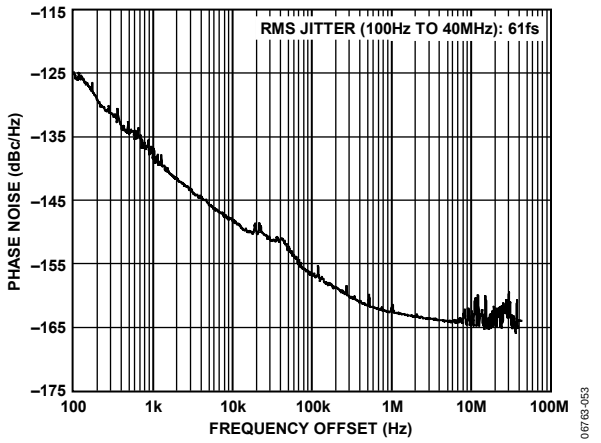

Figure 23. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 171 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

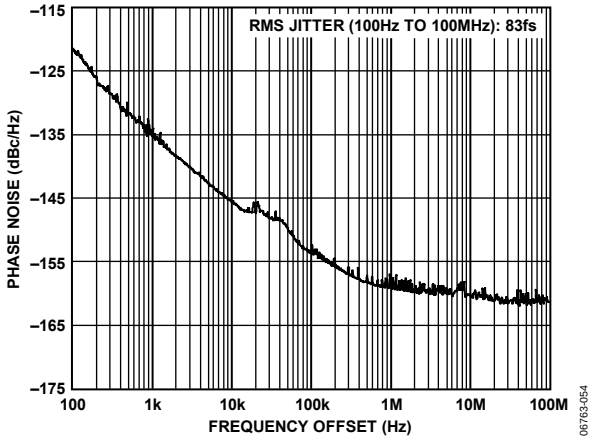

Figure 24. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 258.3 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

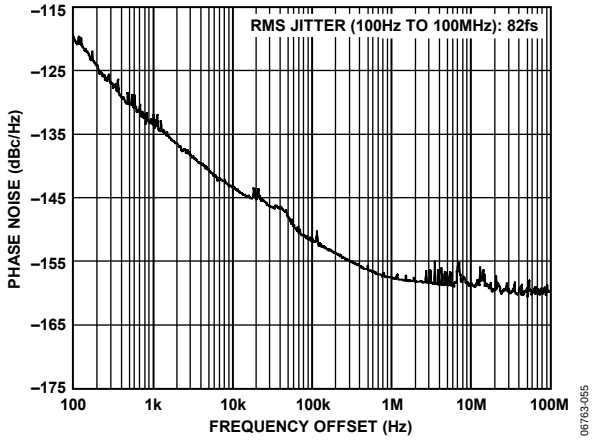

Figure 25. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 311.6 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

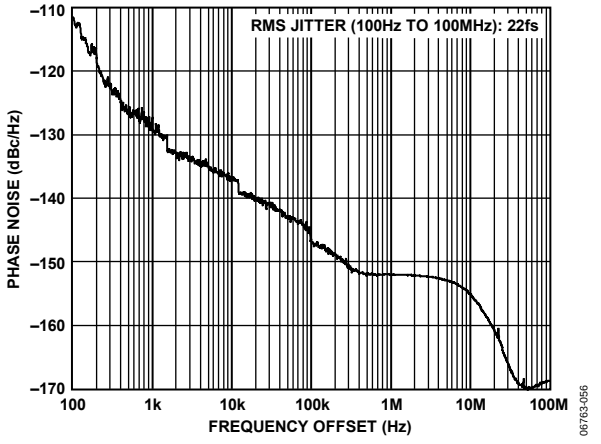

Figure 26. Absolute Phase Noise of 1 GHz Reference Used for Performance Plots; Wenzel Components Used: 100 MHz Oscillator, LNBA-13-24 Amp, LNOM 100-5 Multiplier, LNDD 500-14 Diode Doubler

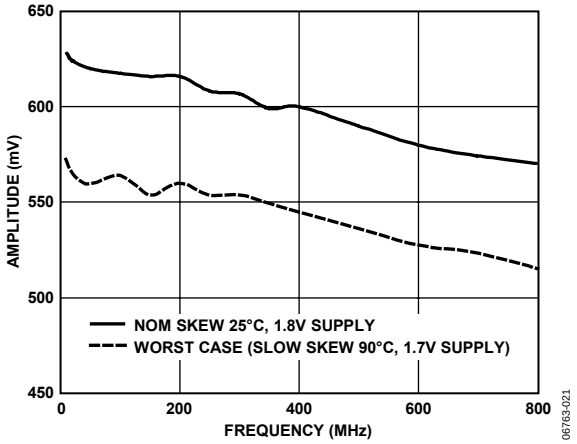

Figure 27. HSTL Output Driver Single-Ended Peak-to-Peak Amplitude vs. Toggle Rate (100 Ω Across Differential Pair)

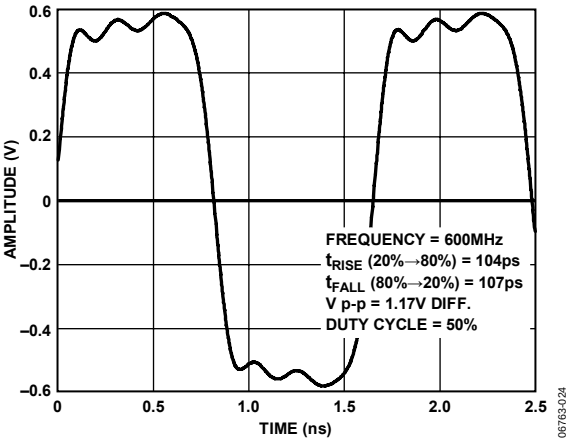

Figure 30. Typical HSTL Output Waveform, Nominal Conditions, DC-Coupled, Differential Probe Across 100 Ω load

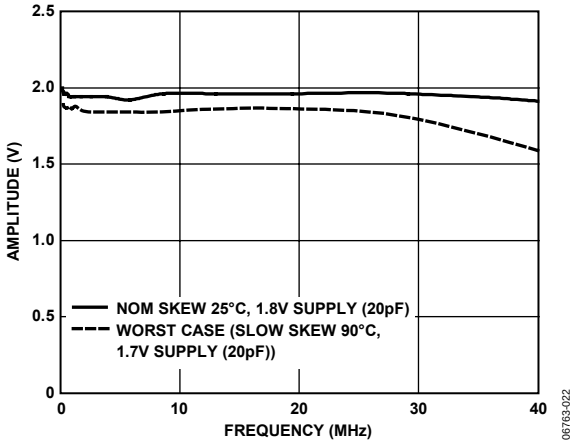

Figure 28. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 1.8 V) with 20 pF Load

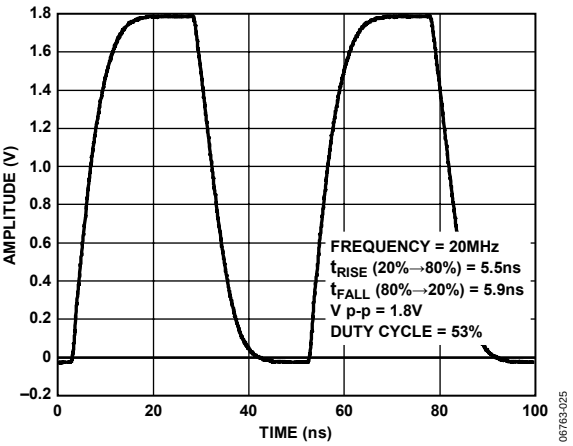

Figure 31. Typical CMOS Output Driver Waveform (@ 1.8 V), Nominal Conditions, Estimated Capacitance = 5 pF

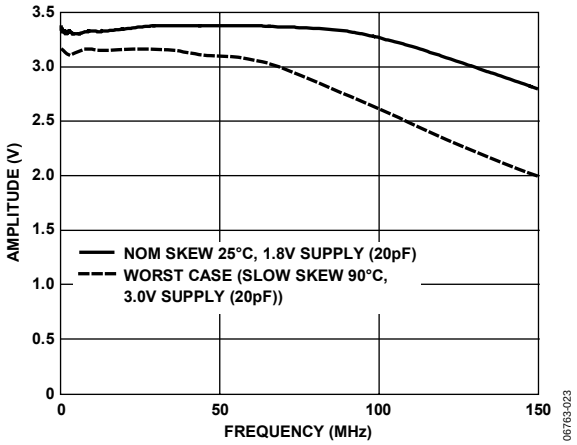

Figure 29. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 3.3 V) with 20 pF Load

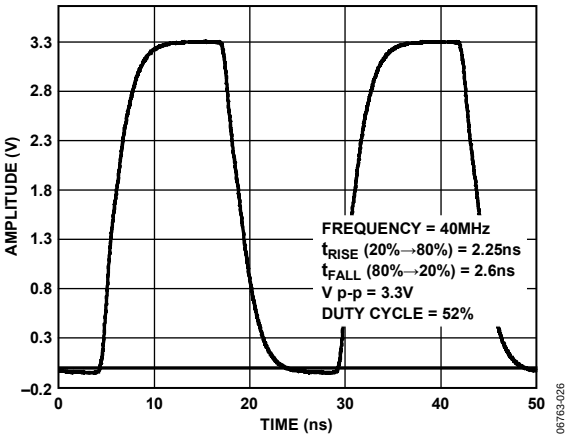

Figure 32. CMOS Output Driver Waveform (@ 3.3 V), Nominal Conditions, Estimated Capacitance = 5 pF

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

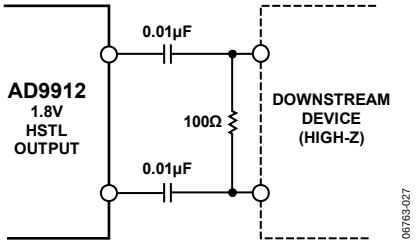

Figure 33. AC-Coupled HSTL Output Driver

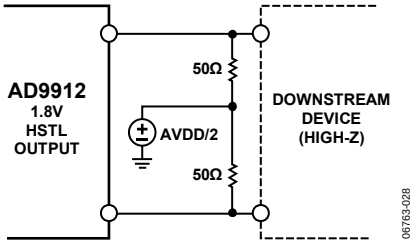

Figure 34. DC-Coupled HSTL Output Driver

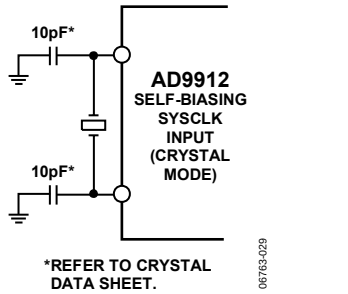

Figure 35. SYSCLK Input, Xtal

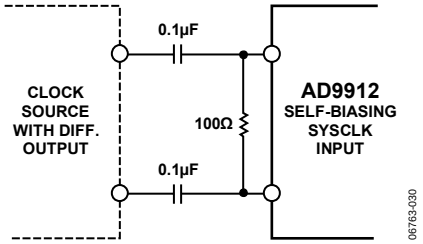

Figure 36. SYSCLK Differential Input, Non-Xtal

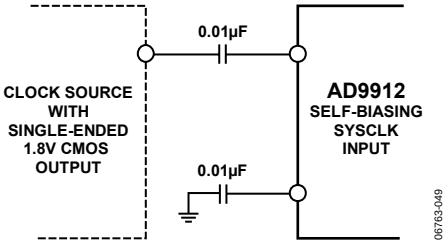

Figure 37. SYSCLK Single-Ended Input, Non-Xtal

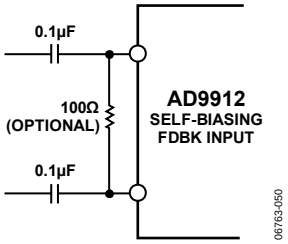

Figure 38. FDBK Input

THEORY OF OPERATION

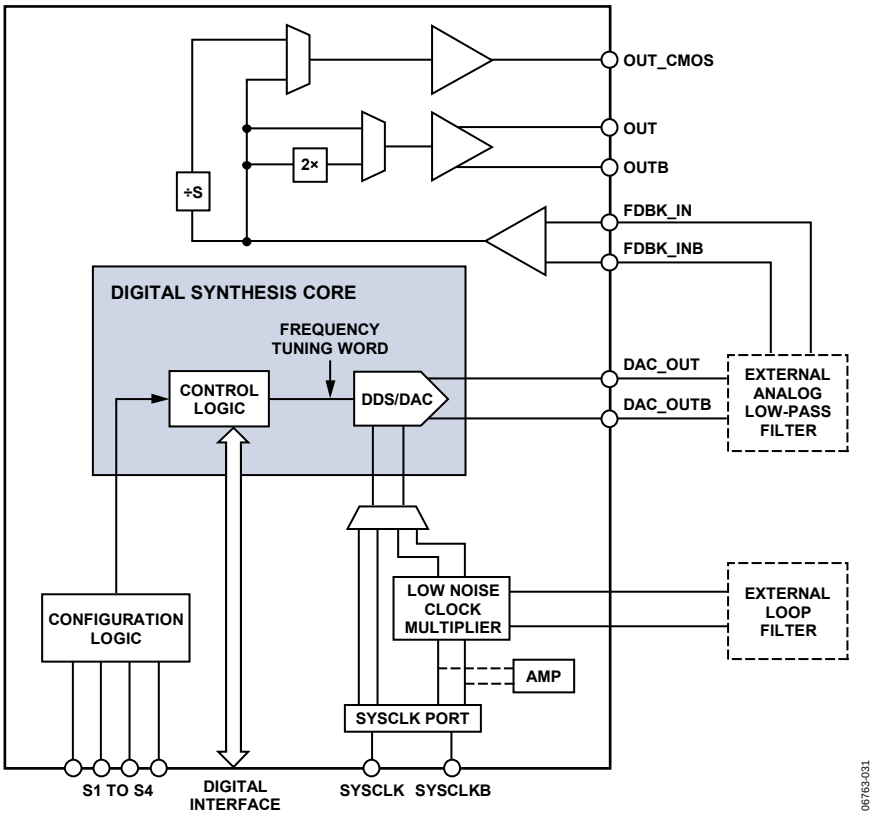

Figure 39. Detailed Block Diagram

OVERVIEW

The AD9912 is a high performance, low noise, 14-bit DDS clock synthesizer with integrated comparators for applications desiring an agile, finely tuned square or sinusoidal output signal. A digitally controlled oscillator (DCO) is implemented using a direct digital synthesizer (DDS) with an integrated output DAC, clocked by the system clock.

A bypassable PLL-based frequency multiplier is present, enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed, and a low noise, high frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter.

The output signal from the reconstruction filter can be fed back to the AD9912 to be processed through the output circuitry.

The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler for applications that need frequencies above the Nyquist level of the DDS.

The AD9912 also offers preprogrammed frequency profiles that allow the user to generate frequencies without programming the part. The individual functional blocks are described in the following sections.

DIRECT DIGITAL SYNTHESIZER

The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{48} counter with a programmable step size (FTW). A block diagram of the DDS is shown in Figure 40.

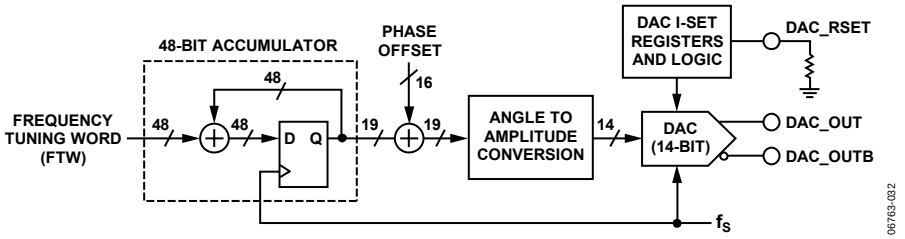

Figure 40. DDS Block Diagram

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output. For example, given an FTW = 5, the accumulator counts by 5s, incrementing on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case), at which point, it rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The next equation defines the average rollover rate of the accumulator and establishes the output frequency (f_{DDS}) of the DDS.

$$f_{DDS} = \left(\frac{FTW}{2^{48}}\right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48}\left(\frac{f_{DDS}}{f_S}\right)\right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 19.44 MHz, then FTW = 5,471,873,547,255 (0x04FA05143BF7).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the phase offset function of the DDS (a programmable 16-bit value (Δphase); see the I/O Register Map section). The resulting phase offset, ΔΦ (radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{16}}\right)$$

DAC OUTPUT

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see the DAC output diagram in Figure 41). The peak output current derives from a combination of two factors. The first is a reference current (I_{DAC_REF}) established at the DAC_RSET pin and the second is a scale factor programmed into the I/O register map.

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2 V nominal, so the reference current can be calculated by

$$I_{DAC\_REF} = \frac{1.2}{R_{DAC\_REF}}$$

Note that the recommended value of I_{DAC_REF} is 120 μA, which leads to a recommended value for R_{DAC_REF} of 10 kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the DAC Full-Scale Current register in the I/O register map. The full-scale DAC output current (I_{DAC_FS}) is given by

$$I_{DAC\_FS} = I_{DAC\_REF}\left(72 + \frac{192FSC}{1024}\right)$$

Using the recommended value of R_{DAC_REF}, the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6 mA to 31.7 mA. 20 mA is the default value.

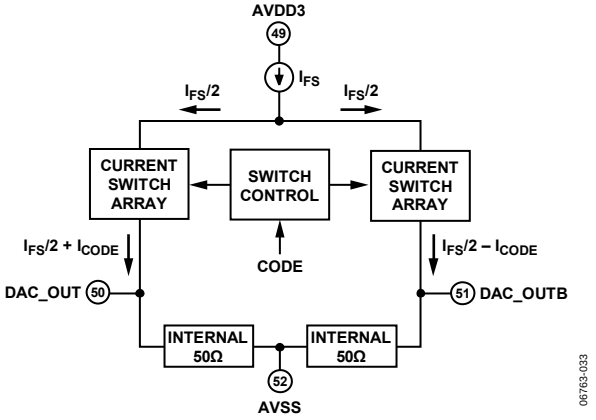

Figure 41. DAC Output

RECONSTRUCTION FILTER

The origin of the output clock signal produced by the AD9912 is the combined DDS and DAC. The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth. If desired, the signal can then be brought back on-chip to be converted to a square wave that is routed internally to the output clock driver or the 2× DLL multiplier.

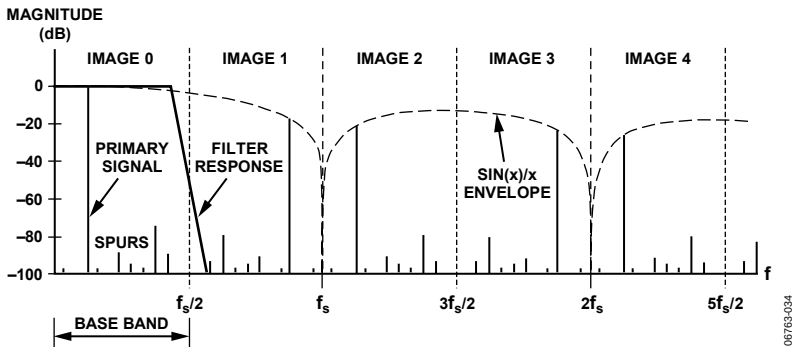

Figure 42. DAC Spectrum vs. Reconstruction Filter Response

Because the DAC constitutes a sampled system, its output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the (typically) desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd images (shown in Figure 42) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample and hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter should preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains significant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a 3rd-, 5th-, or 7th-order elliptic low-pass filter is common.

Some applications operate off an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter.

The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

FDBK INPUTS

The FDBK pins serve as the input to the comparators and output drivers of the AD9912. Typically, these pins are used to receive the signal generated by the DDS after it has been band-limited by the external reconstruction filter.

A diagram of the FDBK input pins is provided in Figure 43, which includes some of the internal components used to bias the input circuitry. Note that the FDBK input pins are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance.

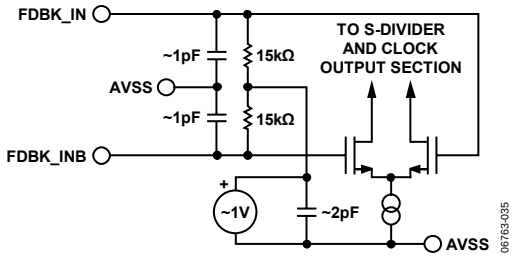

Figure 43. Differential FDBK Inputs

SYSCLK INPUTS

Functional Description

An external time base connects to the AD9912 at the SYSCLK pins to generate the internal high frequency system clock (f_S).

The SYSCLK inputs can be operated in one of three modes:

- SYSCLK PLL bypassed
- SYSCLK PLL enabled with input signal generated externally
- Crystal resonator with SYSCLK PLL enabled

A functional diagram of the system clock generator is shown in Figure 44.

The SYSCLK PLL multiplier path is enabled by a Logic 0 (default) in the PD SYSCLK PLL location of the I/O register map. The SYSCLK PLL multiplier can be driven from the SYSCLK input pins by one of two means, depending on the logic level applied to the 1.8 V CMOS CLKMODESEL pin. When CLKMODESEL = 0, a crystal can be connected directly across the SYSCLK pins. When CLKMODESEL = 1, the maintaining amp is disabled, and an external frequency source (such as an oscillator or signal generator) can be connected directly to the SYSCLK input pins. Note that CLKMODESEL = 1 does not disable the system clock PLL.

The maintaining amp on the AD9912 SYSCLK pins is intended for 25 MHz, 3.2 mm × 2.5 mm AT cut fundamental mode crystals with a maximum motional resistance of 100 Ω. The following crystals, listed in alphabetical order, meet these criteria (as of the revision date of this data sheet):

- AVX/Kyocera CX3225SB
- ECS ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA

Note that while these crystals meet the preceding criteria according to their data sheets, Analog Devices, Inc. does not guarantee their operation with the AD9912, nor does Analog Devices endorse one supplier of crystals over another.

When the SYSCLK PLL multiplier path is disabled, the AD9912 must be driven by a high frequency signal source (250 MHz to 1 GHz). The signal thus applied to the SYSCLK input pins becomes the internal DAC sampling clock (f_S) after passing through an internal buffer.

It is important to note that when bypassing the system clock PLL, the LOOP_FILTER pin (Pin 31) should be pulled down to the analog ground with a 1 kΩ resistor.

SYSCLK PLL Doubler

The SYSCLK PLL multiplier path offers an optional SYSCLK PLL doubler. This block comes before the SYSCLK PLL multiplier and acts as a frequency doubler by generating a pulse on each edge of the SYSCLK input signal. The SYSCLK PLL multiplier locks to the falling edges of this regenerated signal.

The impetus for doubling the frequency at the input of the SYSCLK PLL multiplier is that an improvement in overall phase noise performance can be realized. The main drawback is that the doubler output is not a rectangular pulse with a constant duty cycle even for a perfectly symmetric SYSCLK input signal. This results in a subharmonic appearing at the same frequency as the SYSCLK input signal; and the magnitude of the subharmonic can be quite large. When employing the doubler, care must be taken to ensure that the loop bandwidth of the SYSCLK PLL multiplier adequately suppresses the subharmonic.

The benefit offered by the doubler depends on the magnitude of the subharmonic, the loop bandwidth of the SYSCLK PLL multiplier, and the overall phase noise requirements of the specific application. In many applications, the AD9912 clock output is applied to the input of another PLL, and the subharmonic is often suppressed by the relatively narrow bandwidth of the downstream PLL.

Note that generally, the benefits of the SYSCLK PLL doubler are realized for SYSCLK input frequencies of 25 MHz and above.

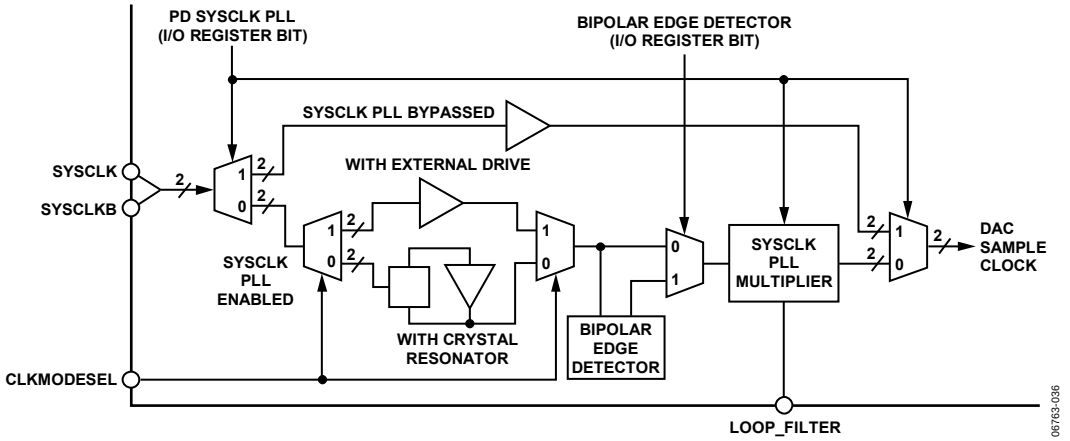

Figure 44. System Clock Generator Block Diagram

SYSCLK PLL Multiplier

When the SYSCLK PLL multiplier path is employed, the frequency applied to the SYSCLK input pins must be limited so as not to exceed the maximum input frequency of the SYSCLK PLL phase detector. A block diagram of the SYSCLK generator appears in Figure 45.

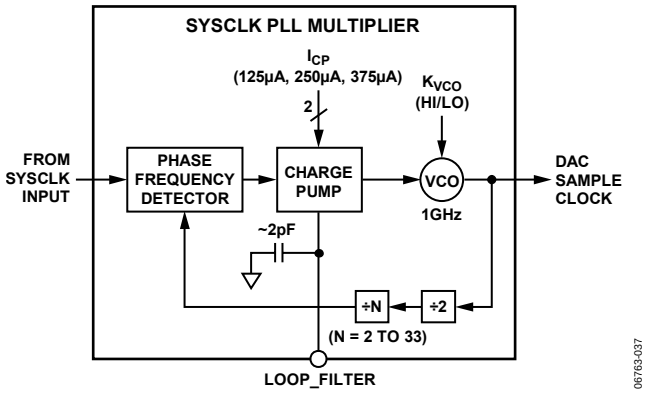

Figure 45. Block Diagram of the SYSCLK PLL

The SYSCLK PLL multiplier has a 1 GHz VCO at its core. A phase/frequency detector (PFD) and charge pump provide the steering signal to the VCO in typical PLL fashion. The PFD operates on the falling edge transitions of the input signal, which means that the loop locks on the negative edges of the reference signal. The charge pump gain is controlled via the I/O register map by selecting one of three possible constant current sources ranging from 125 µA to 375 µA in 125 µA steps. The center frequency of the VCO is also adjustable via the I/O register map and provides high/low gain selection. The feedback path from VCO to PFD consists of a fixed divide-by-2 prescaler followed by a programmable divide-by-N block, where $2 \leq N \leq 33$. This limits the overall divider range to any even integer from 4 to 66, inclusive. The value of N is programmed via the I/O register map via a 5-bit word that spans a range of 0 to 31, but the internal logic automatically adds a bias of 2 to the value entered, extending the range to 33. Care should be taken when choosing these values so as not to exceed the maximum input frequency of the SYSCLK PLL phase detector or SYSCLK PLL doubler. These values can be found in the AC Specifications section.

External Loop Filter (SYSCLK PLL)

The loop bandwidth of the SYSCLK PLL multiplier can be adjusted by means of three external components as shown in Figure 46. The nominal gain of the VCO is 800 MHz/V. The recommended component values (shown in Table 5) establish a loop bandwidth of approximately 1.6 MHz with the charge pump current set to 250 µA. The default case is N = 40 and assumes a 25 MHz SYSCLK input frequency and generates an internal DAC sampling frequency (f_S) of 1 GHz.

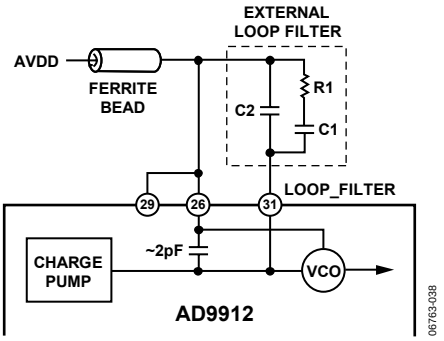

Figure 46. External Loop Filter for SYSCLK PLL

Table 5. Recommended Loop Filter Values for a Nominal 1.5 MHz SYSCLK PLL Loop Bandwidth

Multiplier	R1	Series C1	Shunt C2
<8	390 Ω	1 nF	82 pF
10	470 Ω	820 pF	56 pF
20	1 kΩ	390 pF	27 pF
40 (default)	2.2 kΩ	180 pF	10 pF
60	2.7 kΩ	120 pF	5 pF

Detail of SYSCLK Differential Inputs

A diagram of the SYSCLK input pins is provided in Figure 47. Included are details of the internal components used to bias the input circuitry. These components have a direct effect on the static levels at the SYSCLK input pins. This information is intended to aid in determining how best to interface to the device for a given application.

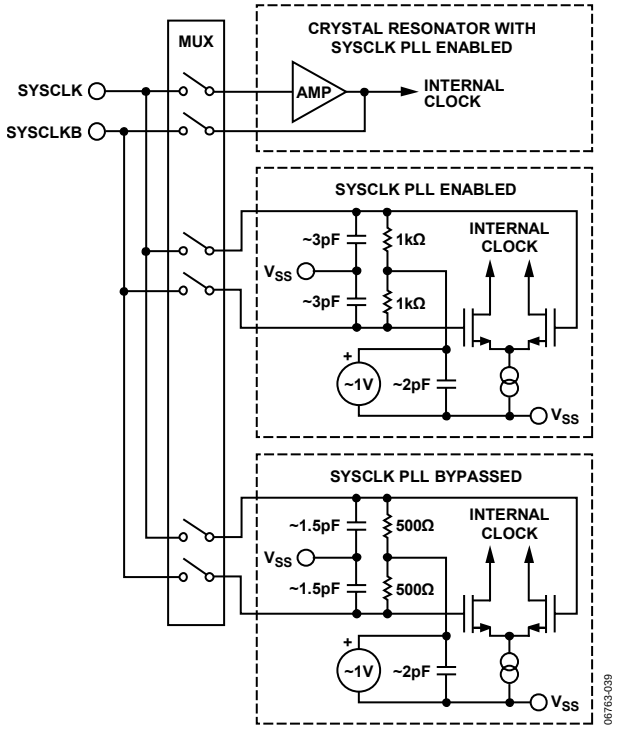

Figure 47. Differential SYSCLK Inputs

Note that the SYSCLK PLL bypassed and SYSCLK PLL enabled input paths are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance. Generally, it is recommended that the SYSCLK inputs be ac-coupled, except when using a crystal resonator.

OUTPUT CLOCK DRIVERS AND 2× FREQUENCY MULTIPLIER

There are two output drivers provided by the AD9912. The primary supports differential 1.8 V HSTL output levels while the secondary supports either 1.8 V or 3.3 V CMOS levels, depending on whether Pin 37 is driven at 1.8 V or 3.3 V.

The primary differential driver nominally provides an output voltage with 100 Ω load applied differentially. The source impedance of the driver is approximately 100 Ω for most of the output clock period; during transition between levels, the source impedance reaches a maximum of about 500 Ω. The driver is designed to support output frequencies of up to and beyond the OC-12 network rate of 622.08 MHz.

The output clock can also be powered down by a control bit in the I/O register map.

Primary 1.8 V Differential HSTL Driver

The DDS produces a sinusoidal clock signal that is sampled at the system clock rate. This DDS output signal is routed off-chip where it is passed through an analog filter and brought back on-chip for buffering and, if necessary, frequency doubling. Where possible, for the best jitter performance, it is recommended that the frequency doubler be bypassed.

The 1.8 V HSTL output should be ac-coupled, with 100 Ω termination at the destination. The driver design has low jitter injection for frequencies in the range of 50 MHz to 750 MHz. Refer to the AC Specifications section for the exact frequency limits.

2× Frequency Multiplier

The AD9912 can be configured (via the I/O register map) with an internal 2× delay-locked loop (DLL) multiplier at the input of the primary clock driver. The extra octave of frequency gain allows the AD9912 to provide output clock frequencies that exceed the range available from the DDS alone. These settings are found in Register 0010 and Register 0200.

The input to the DLL consists of the filtered DDS output signal after it has been squared up by an integrated clock receiver circuit. The DLL can accept input frequencies in the range of 200 MHz to 400 MHz.

Single-Ended CMOS Output

In addition to the high-speed differential output clock driver, the AD9912 provides an independent, single-ended output, CMOS clock driver that is very good for frequencies up to 150 MHz. The signal path for the CMOS clock driver can either include or bypass the CMOS output divider.

If the CMOS output divider is bypassed, the HSTL and CMOS drivers are the same frequency as the signal presented at the FDBK_IN pins. When using the CMOS output in this configuration, the DDS output frequency should be in the range of 30 MHz to 150 MHz. At low output frequencies (<30 MHz), the low slew rate of the DAC results in a higher noise floor. This can be remedied by running the DDS at 100 MHz or greater, and using the CMOS divider. At an output frequency of 50 MHz, the best technique depends on the user's application. Running the DDS at 200 MHz, and using a CMOS divider of 4 results in a lower noise floor, but at the expense of close-in phase noise.

At frequencies greater than 150 MHz, the HSTL output should be used.

CMOS Output Divider (S-Divider)

The CMOS output divider is 16 bits cascaded with an additional divide-by-two. The divider is therefore capable of integer division from 1 to 65,535 (index of 1) or 2 to 131,070 (index of 2). The divider is programmed via the I/O register map to trigger on either the rising (default) or falling edge of the feedback signal.

The CMOS output divider is an integer divider capable of handling frequencies well above the Nyquist limit of the DDS. The S-Divider/2 bit must be set when FDBK_IN is greater than 400 MHz.

Note that the actual output divider values equals the value stored in the output divider register minus one. Therefore, the user would write zeros to the output divider register to have an output divider of one.

HARMONIC SPUR REDUCTION

The most significant spurious signals produced by the DDS are harmonically related to the desired output frequency of the DDS. The source of these harmonic spurs can usually be traced to the DAC, and the spur level is in the −60 dBc range. This ratio represents a level that is about 10 bits below the full-scale output of the DAC (10 bits down is 2^{-10}, or 1/1024).

Such a spur can be reduced by combining the original signal with a replica of the spur but offset in phase by 180°. This idea is the foundation of the technique used to reduce harmonic spurs in the AD9912. Because the DAC has 14-bit resolution, a −60 dBc spur can be synthesized using only the lower 4 bits of the DAC full-scale range. That is, the 4 LSBs can create an output level approximately 60 dB below the full-scale level of the DAC (commensurate with a −60 dBc spur). This fact gives rise to a means of digitally reducing harmonic spurs or their aliased images in the DAC output spectrum by digitally adding a sinusoid at the input of the DAC with a similar magnitude as the offending spur, but shifted in phase to produce destructive interference.

Although the worst spurs tend to be harmonic in origin, the fact that the DAC is part of a sampled system results in the possibility of spurs appearing in the output spectrum that are not harmonically related to the fundamental. For example, if the DAC is sampled at 1 GHz and generates an output sinusoid of 170 MHz, the 5th harmonic would normally be at 850 MHz. However, because of the sampling process, this spur appears at 150 MHz, only 20 MHz away from the fundamental. Therefore, when attempting to reduce DAC spurs it is important to know the actual location of the harmonic spur in the DAC output spectrum based on the DAC sample rate so that its harmonic number can be reduced.

The mechanics of performing harmonic spur reduction is shown in Figure 48. It essentially consists of two additional DDS cores operating in parallel with the original DDS. This enables the user to reduce two different harmonic spurs from the 2nd to the 15th with 9 bits of phase offset control (±π) and 8 bits of amplitude control.

The dynamic range of the cancellation signal is further augmented by a gain bit associated with each channel. When this bit is set, the magnitude of the cancellation signal is doubled by employing a 1-bit left-shift of the data. However, the shift operation reduces the granularity of the cancellation signal magnitude. The full-scale amplitude of a cancellation spur is approximately −60 dBc when the gain bit is a Logic 0 and approximately −54 dBc when the gain bit is a Logic 1.

The procedure for tuning the spur reduction is as follows:

1. Determine which offending harmonic spur to reduce and its amplitude. Enter that harmonic number into Bit 0 to Bit 3 of Register 0x500/Register 0x505.
2. Turn off the fundamental by setting Bit 7 of Register 0x13 and enable the SpurKiller channel by setting Bit 7 of Register 0x500/Register 0x505.
3. Adjust the amplitude of the SpurKiller channel so that it matches the amplitude of the offending spur.
4. Turn the fundamental on by clearing Bit 7 of Register 0x13.
5. Adjust the phase of the SpurKiller channel so that maximum interference is achieved.

Note that the SpurKiller setting is sensitive to the loading of the DAC output pins, and that a DDS reset is required if a SpurKiller channel is turned off. The DDS can be reset by merely setting Bit 0 of Register 0x12, and resetting the part is not necessary.

The performance improvement offered by this technique varies widely and depends on the conditions used. Given this extreme variability, it is impossible to define a meaningful specification to guarantee SpurKiller performance. Current data indicate that a 6 dB to 8 dB improvement is possible for a given output frequency using a common setting over process, temperature, and voltage. There are frequencies, however, where a common setting can result in much greater improvement. Manually adjusting the SpurKiller settings on individual parts can result in more than 30 dB of spurious performance improvement.

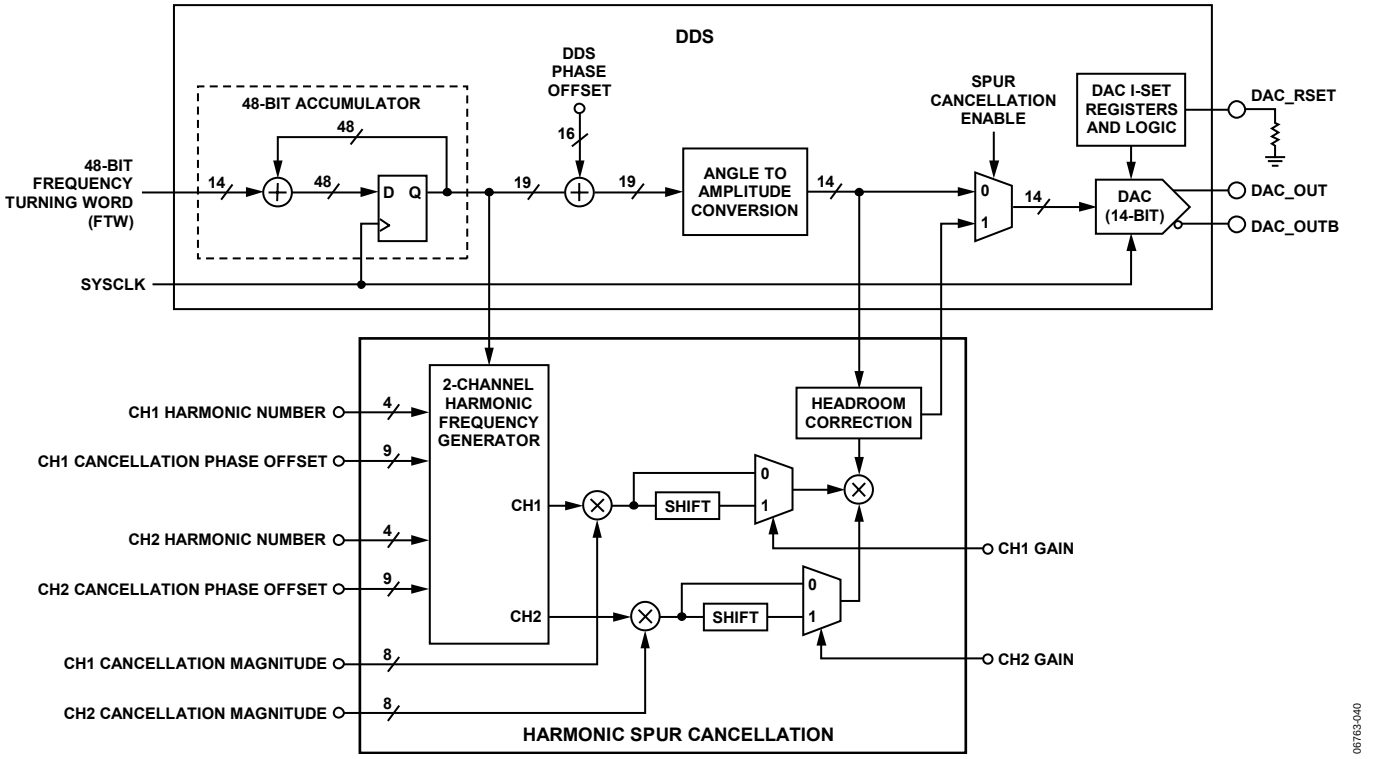

Figure 48. Spur Reduction Circuit Diagram

THERMAL PERFORMANCE

Table 6. Thermal Parameters for AD9912 64-Lead LFCSP Package

Symbol	Thermal Characteristic Using a JEDEC51-7 Plus JEDEC51-5 2S2P Test Board	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/s air flow per JEDEC JESD51-2 (still air)	25.2	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/s air flow per JEDEC JESD51-6 (moving air)	22.0	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.0 m/s air flow per JEDEC JESD51-6 (moving air)	19.8	°C/W
θ_{JB}	Junction-to-board thermal resistance, 1.0 m/s air flow per JEDEC JESD51-8 (moving air)	13.9	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Std 883, Method 1012.1	1.7	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/s air flow per JEDEC JESD51-2 (still air)	0.1	°C/W

The AD9912 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by customer at top center of package.
Ψ_{JT} is the value from Table 6.
PD is the power dissipation (see the Total Power Dissipation section in the Specifications section).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

AD9912 POWER-UP

POWER-ON RESET

On initial power-up, the AD9912 internally generates a 75 ns RESET pulse. The pulse is initiated when both of the following two conditions are met:

- The 3.3 V supply is greater than 2.35 ± 0.1 V.
- The 1.8 V supply is greater than 1.4 ± 0.05 V.

Less than 1 ns after RESET goes high, the S1 to S4 configuration pins go high impedance and remain high impedance until RESET is deactivated. This allows strapping and configuration during RESET.

Because of this reset sequence, external power supply sequencing is not critical.

DEFAULT OUTPUT FREQUENCY ON POWER-UP

The four status pins (S1 to S4) are used to define the output frequency of the DDS at power-up even though the I/O registers have not yet been programmed. At power-up, internal logic initiates a reset pulse of about 10 ns. During this time, S1 to S4 briefly function as input pins and can be driven externally. Any logic levels thus applied are transferred to a 4-bit register on the falling edge of the internally initiated pulse. The same behavior occurs when the RESET pin is asserted manually.

Setting up S1 to S4 for default DDS startup is accomplished by connecting a resistor to each pin (either pull-up or pull-down) to produce the desired bit pattern, yielding 16 possible states that are used both to address an internal 8 × 16 ROM and to select the SYSCLK mode (see Table 7). The ROM contains eight 16-bit DDS frequency tuning words (FTWs), one of which is selected by the state of the S1 to S3 pins. The selected FTW is transferred to the FTW0 register in the I/O register map without the need for an I/O update. This ensures that the DDS generates the selected frequency even if the I/O registers have not been programmed. The state of the S4 pin selects whether the internal system clock is generated by means of the internal SYSCLK PLL multiplier or not (see the SYSCLK Inputs section for details).

The DDS output frequency listed in Table 7 assumes that the internal DAC sampling frequency (f_S) is 1 GHz. These frequencies scale 1:1 with f_S, meaning that other start-up frequencies are available by varying the SYSCLK frequency.

At startup, the internal frequency multiplier defaults to 40× when the Xtal/PLL mode is selected via the status pins.

Table 7. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

POWER SUPPLY PARTITIONING

The AD9912 features multiple power supplies, and their power consumption varies with its configuration. This section covers which power supplies can be grouped together and how the power consumption of each block varies with frequency.

The numbers quoted here are for comparison only. Refer to the Specifications section for exact numbers. With each group, bypass capacitors of 1 µF in parallel with a 10 µF should be used.

The recommendations here are for typical applications, and for these applications, there are four groups of power supplies: 3.3 V digital, 3.3 V analog, 1.8 V digital, and 1.8 V analog.

Applications demanding the highest performance may require additional power supply isolation.

3.3 V SUPPLIES

DVDD_I/O (Pin 1) and AVDD3 (Pin 14)

Even though one of these pins is analog, and the other digital, these two 3.3 V supplies can be grouped together. The power consumption on Pin 1 varies dynamically with serial port activity.

AVDD3 (Pin 37)

This is the CMOS driver supply and can be either 1.8 V or 3.3 V, and its power consumption is a function of the output frequency and loading of OUT_CMOS (Pin 38).

If the CMOS driver is used at 3.3 V, this supply should be isolated from other 3.3 V supplies with a ferrite bead to avoid a spur at the output frequency. If the HSTL driver is not used, AVDD3 (Pin 37) can be connected (using a ferrite bead) to AVDD3 (Pin 46, Pin 47, Pin 49). If the HSTL driver is used, connect AVDD3 (Pin 37) using a ferrite bead to Pin 1 and Pin 14.

If the CMOS driver is used at 1.8 V, AVDD3 (Pin 37) can be connected to AVDD (Pin 36).

If the CMOS driver is not used, AVDD3 (Pin 37) can be tied directly to the 1.8 V AVDD (Pin 36) and the CMOS driver powered down using Register 0010.

AVDD3 (Pin 46, Pin 47, and Pin 49)

These are 3.3 V DAC power supplies that typically consume about 25 mA. At a minimum, a ferrite bead should be used to isolate these from other 3.3 V supplies, with a separate regulator being ideal.

1.8 V SUPPLIES

DVDD (Pin 3, Pin 5, and Pin 7)

These pins should be grouped together and isolated from the 1.8 V AVDD supplies. A separate regulator should be used. A ferrite bead can be used for applications where spurious performance is not critical. Their current consumption increases from about 160 mA at a system clock of 700 MHz to about 205 mA at a system clock of 1 GHz. There is also a slight (~5%) increase as f_{OUT} increases from 50 MHz to 400 MHz.

AVDD (Pin 11, Pin 19, Pin 23, Pin 24, Pin 36, Pin 42, Pin 44, and Pin 45)

These pins can be grouped together and should be isolated from other 1.8 V supplies. A separate regulator is recommended. At a minimum, a ferrite bead should be used for isolation.

AVDD (Pin 53)

This 1.8 V supply consumes about 40 mA. The supply can be run off the same regulator as 1.8 V AVDD group, with a ferrite bead to isolate Pin 53 from the rest of the 1.8 V AVDD group. However, for applications demanding the highest performance, a separate regulator is recommended.

AVDD (Pin 25, Pin 26, Pin 29, and Pin 30)

These system clock PLL power pins should be grouped together and isolated from other 1.8 V AVDD supplies by having these four pins on their own LDO. It is recommended to isolate Pin 25 and Pin 30 from Pin 26 and Pin 29 using a ferrite bead.

At a minimum, it is recommended to tie Pin 25 and Pin 30 together and to isolate them from the aggregate AVDD 1.8 V supply with a ferrite bead. Likewise, Pin 26 and Pin 29 can also be tied together, with a ferrite bead isolating them from the same aggregate 1.8 V supply. The loop filter for the system clock PLL should directly connect to Pin 26 and Pin 29 (see Figure 46).

If the system clock PLL is bypassed, the loop filter pin (Pin 31) should be pulled down to analog ground using a 1 kΩ resistor.

SERIAL CONTROL PORT

The AD9912 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9912 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin has an internal pull-down resistor.

SDIO (serial data input/output) is a dual-purpose pin and acts as input only or input/output. The AD9912 defaults to bidirectional pins for I/O. Alternatively, SDIO can be used as a unidirectional I/O pin by writing to the SDO Active bit at Register 0000[7] = 1. In this case, SDIO is the input, and SDO is the output.

SDO (serial data out) is used only in the unidirectional I/O mode (Register 0000[7] = 1) as a separate output pin for reading back data. Bidirectional I/O mode (using SDIO as both input and output) is active by default (SDO enable register at Register 0000[7] = 0).

CSB (chip select bar) is an active low control that gates the read and write cycles. When CSB is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 100 kΩ resistor to 3.3 V. It should not be left floating. See the Operation of Serial Control Port section on the use of the CSB in a communication cycle.

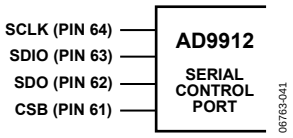

Figure 49. Serial Control Port

OPERATION OF SERIAL CONTROL PORT

Framing a Communication Cycle with CSB

A communication cycle (a write or a read operation) is gated by the CSB line. CSB must be brought low to initiate a communication cycle.

CSB stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (W1:W0 must be set to 00, 01, or 10; see Table 8). In these modes, CSB can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. CSB can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer. During this period, the serial control port state machine enters a wait state until all data has been sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfer or by returning the CSB low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). Raising the CSB on a non-byte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (W1:W0 = 11), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). CSB must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9912. The first writes a 16-bit instruction word into the AD9912, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9912 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation (I15 = 0), the second part is the transfer of data into the serial control port buffer of the AD9912. The length of the transfer (1, 2, 3 bytes, or streaming mode) is indicated by 2 bits (W1:W0) in the instruction byte. The length of the transfer indicated by W1:W0 does not include the 2-byte instruction. CSB can be raised after each sequence of 8 bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when CSB is lowered. Stalling on non-byte boundaries resets the serial control port.

There are three types of registers on the AD9912: buffered, live, and read-only. Buffered (also referred to as mirrored) registers require an I/O update to transfer the new values from a temporary buffer on the chip to the actual register and are marked with an M in the column labeled Type of the register map. Toggling the IO_UPDATE pin or writing a 1 to the Register Update bit (Register 0005[0]) causes the update to occur. Because any number of bytes of data can be changed before issuing an update command, the update simultaneously enables all register changes since any previous update. Live registers do not require I/O update and update immediately after being written. Read-only registers ignore write commands and are marked RO in the Type column of the register map. The Type column of the register map may also have an AC, which indicates that the register is auto-clearing.

Read

If the instruction word is for a read operation (I15 = 1), the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1, 2, 3, 4 as determined by W1:W0. In this case, 4 is used for streaming mode where 4 or more words are transferred per read. The data readback is valid on the falling edge of SCLK.

The default mode of the AD9912 serial control port is bidirectional mode, and the data readback appears on the SDIO pin. It is possible to set the AD9912 to unidirectional mode by writing the SDO enable register at Register 0000[7] = 0, and in that mode, the requested data appears on the SDO pin.

By default, a read request reads the register value that is currently in use by the AD9912. However, setting Register 0004[0] = 1 causes the buffered registers to be read instead. The buffered registers are the ones that take effect during the next I/O update.

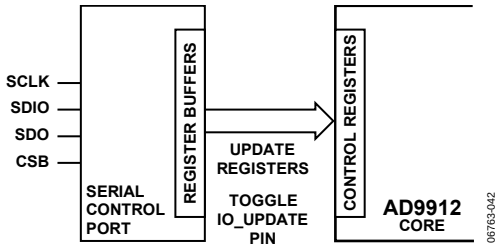

Figure 50. Relationship Between Serial Control Port Register Buffers and Control Registers of the AD9912

The AD9912 uses Register 0000 to Register 0509. Although the AD9912 serial control port allows both 8-bit and 16-bit instructions, the 8-bit instruction mode provides access to five address bits (A4 to A0) only, which restricts its use to the address space 0x00 to 0x01. The AD9912 defaults to 16-bit instruction mode on power-up, and the 8-bit instruction mode is not supported.

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1:W0, are the transfer length in bytes. The final 13 bits are the address (A12:A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits [W1:W0], which is interpreted according to Table 8.

Bits [A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. The AD9912 uses all of the 13-bit address space. For multibyte transfers, this address is the starting byte address.

Table 8. Byte Transfer Count

W1	W0	Bytes to Transfer (Excluding the 2-Byte Instruction)
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

MSB/LSB FIRST TRANSFERS

The AD9912 instruction word and byte data can be MSB first or LSB first. The default for the AD9912 is MSB first. The LSB first mode can be enabled by writing a 1 to the LSB First bit in the Serial Configuration register and then issuing an I/O update. Immediately after the LSB first bit is set, all serial control port operations are changed to LSB first order.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from high address to low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB First = 1 (LSB first), the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial control port internal byte address generator increments for each byte of the multibyte transfer cycle.

The AD9912 serial control port register address decrements from the register address just written toward 0x0000 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the serial control port register address increments from the address just written toward 0x1FFF for multibyte I/O operations.

Unused addresses are not skipped during multibyte I/O operations. The user should write the default value to a reserved register and should only write zeros to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 9. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

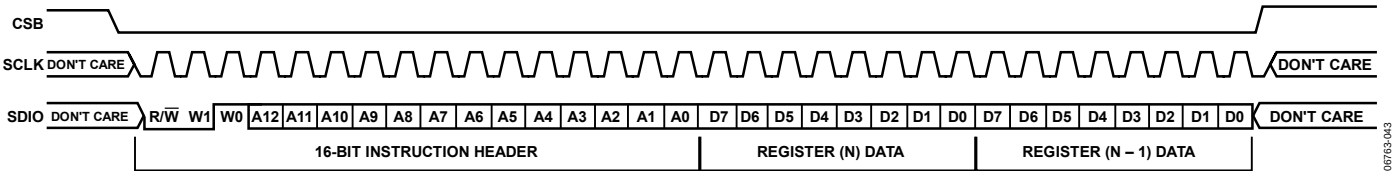

Figure 51. Serial Control Port Write—MSB First, 16-Bit Instruction, 2 Bytes Data

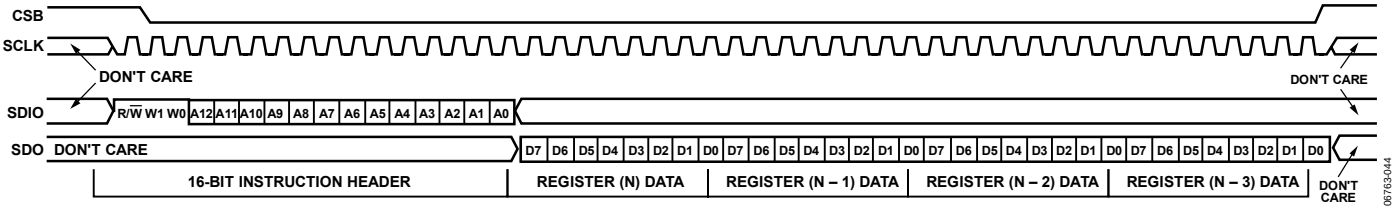

Figure 52. Serial Control Port Read—MSB First, 16-Bit Instruction, 4 Bytes Data

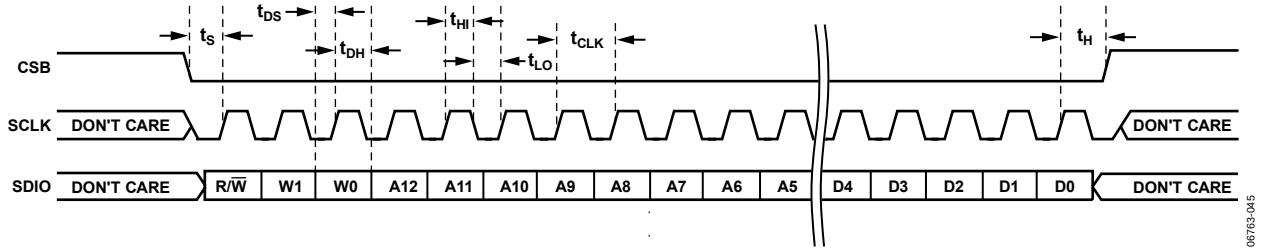

Figure 53. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

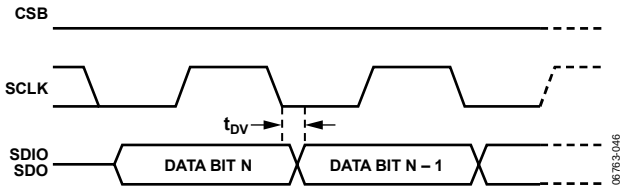

Figure 54. Timing Diagram for Serial Control Port Register Read

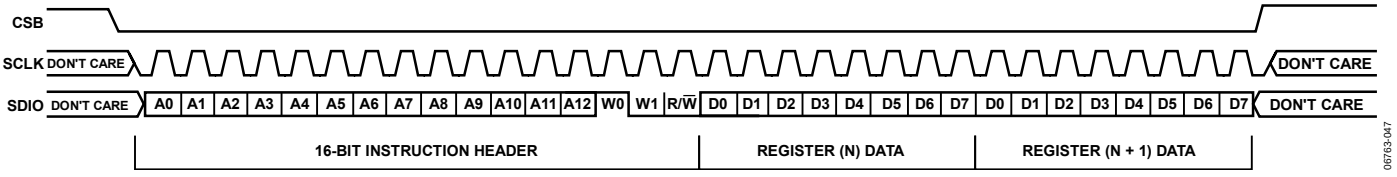

Figure 55. Serial Control Port Write—LSB First, 16-Bit Instruction, 2 Bytes Data

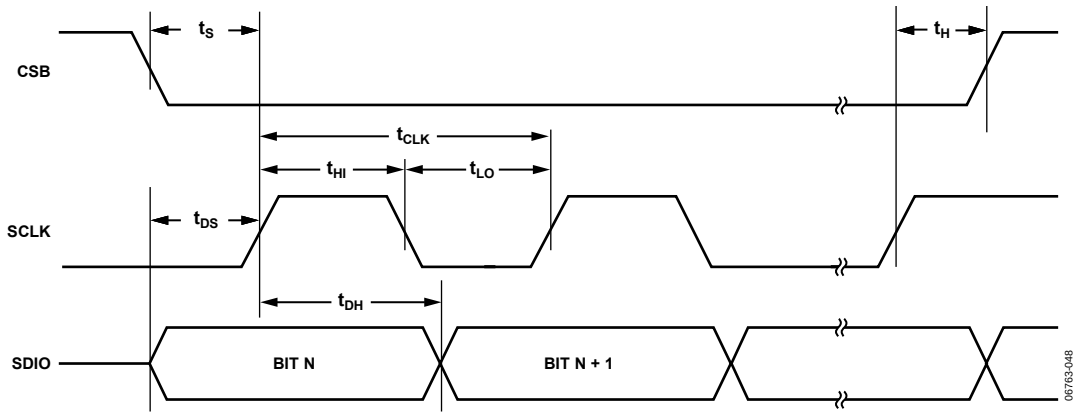

Figure 56. Serial Control Port Timing—Write

Table 10. Definitions of Terms Used in Serial Control Port Timing Diagrams

Parameter	Description
t_{CLK}	Period of SCLK
t_{DV}	Read data valid time (time from falling edge of SCLK to valid data on SDIO/SDO)
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

I/O REGISTER MAP

Table 11.

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Serial Port Configuration and Part Identification											
0000		Serial Config.	SDO Active	LSB First (buffered)	Soft Reset	Long Inst.					18
0001		Reserved									00
0002	RO	Part ID	Part ID								02
0003	RO										09
0004		Serial Options								Read Buffer Reg.	00
0005	AC									Register Update	00
Power-Down and Reset											
0010		Power-Down and Enable	PD HSTL Driver	Enable CMOS Driver	Enable Output Doubler	PD SYSCLK PLL			Full PD	Digital PD	C0 or D0
0011		Reserved									00
0012	M, AC	Reset								DDS Reset	00
0013	M		PD Fund DDS				S Div2 Reset		S-Divider Reset		00
System Clock											
0020		N-Divider				N-Divider [4:0]					12
0021		Reserved									00
0022		PLL Parameters	VCO Auto Range				2× Refer-ence	VCO Range	Charge Pump Current [1:0]		04
CMOS Output Divider (S-Divider)											
0100		Reserved									30
0101 to 0103		Reserved									00
0104 to 0105		S-Divider	S-Divider [15:0] LSB: Register 0104								00
0106			Falling Edge Triggered							S-Divider/2	01
Frequency Tuning Word											
01A0 to 01A5		Reserved									00
01A6	M	FTW0 (Frequency Tuning Word)	FTW0 [47:0] LSB: Register 01A6								00
01A7	M										00
01A8	M										00
01A9	M										00
01AA	M										Start-up cond.
01AB	M										Start-up cond.
01AC to 01AD	M	Phase	DDS Phase Word [15:0]								00

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Doubler and Output Drivers											
0200		HSTL Driver				OPOL (polarity)			HSTL Output Doubler [1:0]		05
0201		CMOS Driver								CMOS MUX	00
Calibration (User-Accessible Trim)											
0400 to 040A		Reserved									00
040B		DAC Full-Scale Current	DAC Full-Scale Current [7:0]								FF
040C									DAC Full-Scale Current [9:8]		01
040D		Reserved									00
040E		Reserved									10
040F to 0410		Reserved									00
Harmonic Spur Reduction											
0500	M	Spur A	HSR-A Enable	Amplitude Gain × 2			Spur A Harmonic [3:0]				00
0501	M		Spur A Magnitude [7:0]								00
0503	M		Spur A Phase [7:0]								00
0504	M									Spur A Phase [8]	00
0505	M	Spur B	HSR-B Enable	Amplitude Gain × 2			Spur B Harmonic [3:0]				00
0506	M		Spur B Magnitude [7:0]								00
0508	M		Spur B Phase [7:0]								00
0509	M									Spur B Phase [8]	00

[1] Types of registers: M = mirrored (also called buffered). This type of register needs an I/O update for the new value to take effect; RO = read-only; AC = auto-clear.

I/O REGISTER DESCRIPTION

SERIAL PORT CONFIGURATION (REG 0000 TO REG 0005)

Register 0000—Serial Configuration

Table 12.

Bits	Bit Name	Description
D0	SDO Active	Enables SDO Pin. 1 = SDO pin enabled (4-wire serial port mode). 0 = 3-wire mode.
D1	LSB First	Sets bit order for serial port. 1 = LSB first. 0 = MSB first. I/O update must occur in order to take effect.
D2	Soft Reset	Resets register map, except for Register 0000. Setting this bit forces a soft reset, meaning that S1 to S4 are not tristated, nor is their state read when this bit is cleared. The AD9912 assumes the values of S1 to S4 that were present during the last hard reset. This bit is not self-clearing, and all other registers are restored to their default values after a soft reset.
D3	Long Instruction	Read-only: this part only supports long instructions.
D4:D7		These bits are the mirror image of Bits [D0:D3].

Register 0001—Reserved

Register 0002 to Register 0003—Part ID (Read-Only)

Register 0004—Serial Options

Table 13.

Bits	Bit Name	Description
D0	Read Buffer Register	For buffered registers, serial port read-back reads from actual (active) registers instead of the buffer. 1 = reads the buffered values that take effect during the next I/O update. 0 = reads values that are currently in effect.

Register 0005—Serial Options (Self Clearing)

Table 14.

Bits	Bit Name	Description
D0	Register Update	Software access to the register update pin function. Writing a 1 to this bit is identical to performing an I/O update.

POWER-DOWN AND RESET (REG 0010 TO REG 0013)

Register 0010—Power-Down and Enable

Power-up default is defined by start-up pins.

Table 15.

Bits	Bit Name	Description
D0	Digital PD	Removes clock from most of digital section; leave serial port usable. In contrast to full PD, setting this bit does not debias inputs, allowing for quick wake-up.
D1	Full PD	Setting this bit is identical to activating the PD pin and puts all blocks (except serial port) into power-down mode. SYSCLK is turned off.
D4	PD SYSCLK PLL	System clock multiplier power-down. 1 = system clock multiplier powered down. If the S4 pin is tied high at power-up or reset, this bit is set, and the default value for Register 0010 is D0, not C0.
D5	Enable Output Doubler	Powers up output clock generator doubler. Output doubler must still be enabled in Register 0200.
D6	Enable CMOS Driver	Powers up CMOS output driver. 1 = CMOS driver on.
D7	PD HSTL Driver	Powers down HSTL output driver. 1 = HSTL driver powered down.

Register 0011—Reserved

Register 0012—Reset (Auto-Clear)

To reset the entire chip, the user can use the (non-self clearing) Soft Reset bit in Register 0000.

Table 16.

Bits	Bit Name	Description
D0	DDS Reset	Reset of the direct digital synthesis block. Reset of this block is very seldom needed.

Register 0013—Reset (Continued) (Not Auto-Clear)

Table 17.

Bits	Bit Name	Description
D1	S-Divider Reset	Synchronous (to S-divider prescaler output) reset for integer divider.
D3	S Div2 Reset	Asynchronous reset for S prescaler.
D7	PD Fund DDS	Setting this bit powers down the DDS fundamental output but not the spurs. It is used during tuning of the SpurKiller circuit.

SYSTEM CLOCK (REG 0020 TO REG 0022)

Register 0020—N-Divider

Table 18.

Bits	Bit Name	Description
D4:D0	N-Divider	These bits set the feedback divider for system clock PLL. There is a fixed divide-by-2 preceding this block, as well as an offset of 2 added to this value. Therefore, setting this register to 00000 translates to an overall feedback divider ratio of 4. See Figure 45.

Register 0021—Reserved

Register 0022—PLL Parameters

Table 19.

Bits	Bit Name	Description
D1:D0	Charge Pump Current	Charge pump current. 00 = 250 µA. 01 = 375 µA. 10 = off. 11= 125 µA.
D2	VCO Range	Selects low range or high range VCO. 0 = low range (700 MHz to 810 MHz). 1 = high range (900 MHz to 1000 MHz). For system clock settings between 810 MHz and 900 MHz, use the VCO Auto Range (Bit 7) to set the correct VCO range automatically.
D2	2× Reference	Enables a frequency doubler prior to the SYSCLK PLL and can be useful in reducing jitter induced by the SYSCLK PLL. See Figure 44.
D4:D6	Reserved	
D7	VCO Auto Range	Automatic VCO range selection. Enabling this bit allows Bit 2 of this register to be set automatically.

CMOS OUTPUT DIVIDER (S-DIVIDER) (REG 0100 TO REG 0106)

Register 0100 to Register 0103—Reserved

Register 0104 to Register 0105—S-Divider

Table 20.

Bits	Bit Name	Description
D15:D0	S-Divider	CMOS output divider. Divide ratio = 1 − 65,536. If the desired S-divider setting is greater than 65,536, or if the signal on FDBK_IN is greater than 400 MHz, then Bit 0, Register 0106 must be set. Note that the actual S-divider is the value in this register plus 1; so to have an S-divider of 1, Register 0104 and Register 0105 must both be 0x00. Register 104 is the least significant byte.

Register 0106—S-Divider (Continued)

Table 21.

Bits	Bit Name	Description
D0	S-Divider/2	Setting this bit enables an additional /2 prescaler. See the CMOS Output Divider (S-Divider) section. If the desired S-divider setting is greater than 65,536, or if the signal on FDBK_IN is greater than 400 MHz, this bit must be set.
D6:D1	Reserved	
D7	Falling Edge Triggered	Setting this bit inverts the reference clock before S-divider.

FREQUENCY TUNING WORD (REG 01A0 TO REG 01AD)

Register 01A0 to Register 01A5—Reserved

Register 01A6 to Register 01AB—FTW0

Table 22.

Bits	Bit Name	Description
D47:D0	FTW0	These registers contain the FTW (frequency tuning word) for the DDS. The FTW determines the ratio of the AD9912 output frequency to its DAC system clock. Register 01A6 is the least significant byte of the FTW. Note that the power-up default is defined by start-up Pin S1 to Pin S4.

Register 01AC to Register 01AD—Phase

Table 23.

Bits	Bit Name	Description
D15:D0	DDS Phase Word	Allows user to vary the phase of the DDS output. See the Direct Digital Synthesizer section.

DOUBLER AND OUTPUT DRIVERS (REG 0200 TO REG 0201)

Register 0200—HSTL Driver

Table 24.

Bits	Bit Name	Description
D1:D0	HSTL Output Doubler	HSTL output doubler. 01 = doubler disabled. 10 = doubler enabled. When using doubler, Register 0010[5] must also be set to 1.
D3:D2	Reserved	
D4	OPOL	Output polarity. Setting this bit inverts the HSTL driver output polarity.

Register 0201—CMOS Driver

Table 25.

Bits	Bit Name	Description
D0	CMOS Mux	This bit allows the user to select whether the CMOS driver output is divided by the S-divider. 0 = S-divider input sent to CMOS driver. 1 = S-divider output sent to CMOS driver. See Figure 39.

CALIBRATION (USER-ACCESSIBLE TRIM) (REG 0400 TO REG 0410)

Register 0400 to Register 040A—Reserved

Register 040B—DAC Full-Scale Current

Table 26.

Bits	Bit Name	Description
D7:D0	DAC Full-Scale Current	DAC Full-Scale Current [7:0]. See the DAC Output section.

Register 040C—DAC Full-Scale Current (Continued)

Table 27.

Bits	Bit Name	Description
D1:D0	DAC Full-Scale Current	DAC Full-Scale Current [9:8]. See Register 040B.

Register 040D to Register 0410—Reserved

HARMONIC SPUR REDUCTION (REG 0500 TO REG 0509)

See the Harmonic Spur Reduction section.

Register 0500—Spur A

Table 28.

Bits	Bit Name	Description
D3:D0	Spur A Harmonic	Spur A Harmonic 1 to 15. Allows user to choose which harmonic to eliminate.
D5:D4	Reserved	
D6	Amplitude Gain × 2	Setting this bit doubles the gain of the cancelling circuit, but also doubles the minimum step size.
D7	HSR-A Enable	Harmonic Spur Reduction A enable.

Register 0501—Spur A (Continued)

Table 29.

Bits	Bit Name	Description
D7:D0	Spur A Magnitude	Linear multiplier for Spur A magnitude.

Register 0503 to Register 0504—Spur A (Continued)

Table 30.

Bits	Bit Name	Description
D8	Spur A Phase	Linear offset for Spur A phase.

Register 0505—Spur B

Table 31.

Bits	Bit Name	Description
D3:D0	Spur B Harmonic	Spur B Harmonic 1 to 15. Allows user to choose which harmonic to eliminate.
D5:D4	Reserved	
D6	Amplitude Gain × 2	Setting this bit doubles the gain of the cancelling circuit, but also doubles the minimum step size.
D7	HSR-B Enable	Harmonic Spur Reduction B enable.

Register 0506—Spur B (Continued)

Table 32.

Bits	Bit Name	Description
D7:D0	Spur B Magnitude	Linear multiplier for Spur B magnitude.

Register 0508 to Register 0509—Spur B (Continued)

Table 33.

Bits	Bit Name	Description
D8	Spur B Phase	Linear offset for Spur B phase.

OUTLINE DIMENSIONS

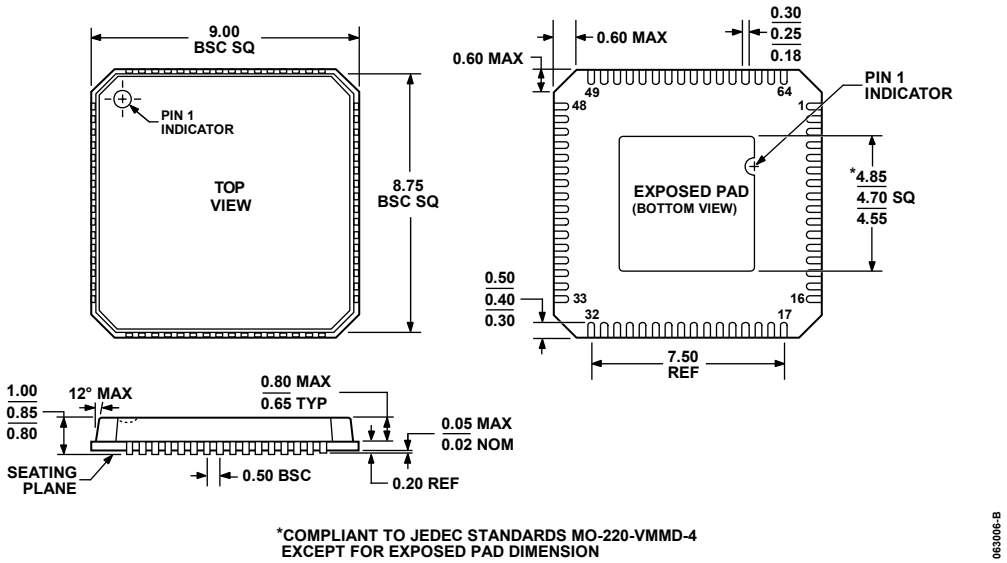

Figure 57. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9912BCPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9912BCPZ-REEL7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9912/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

D06763-0-1/08(A)